Programmable Interval Timer

8253

By,

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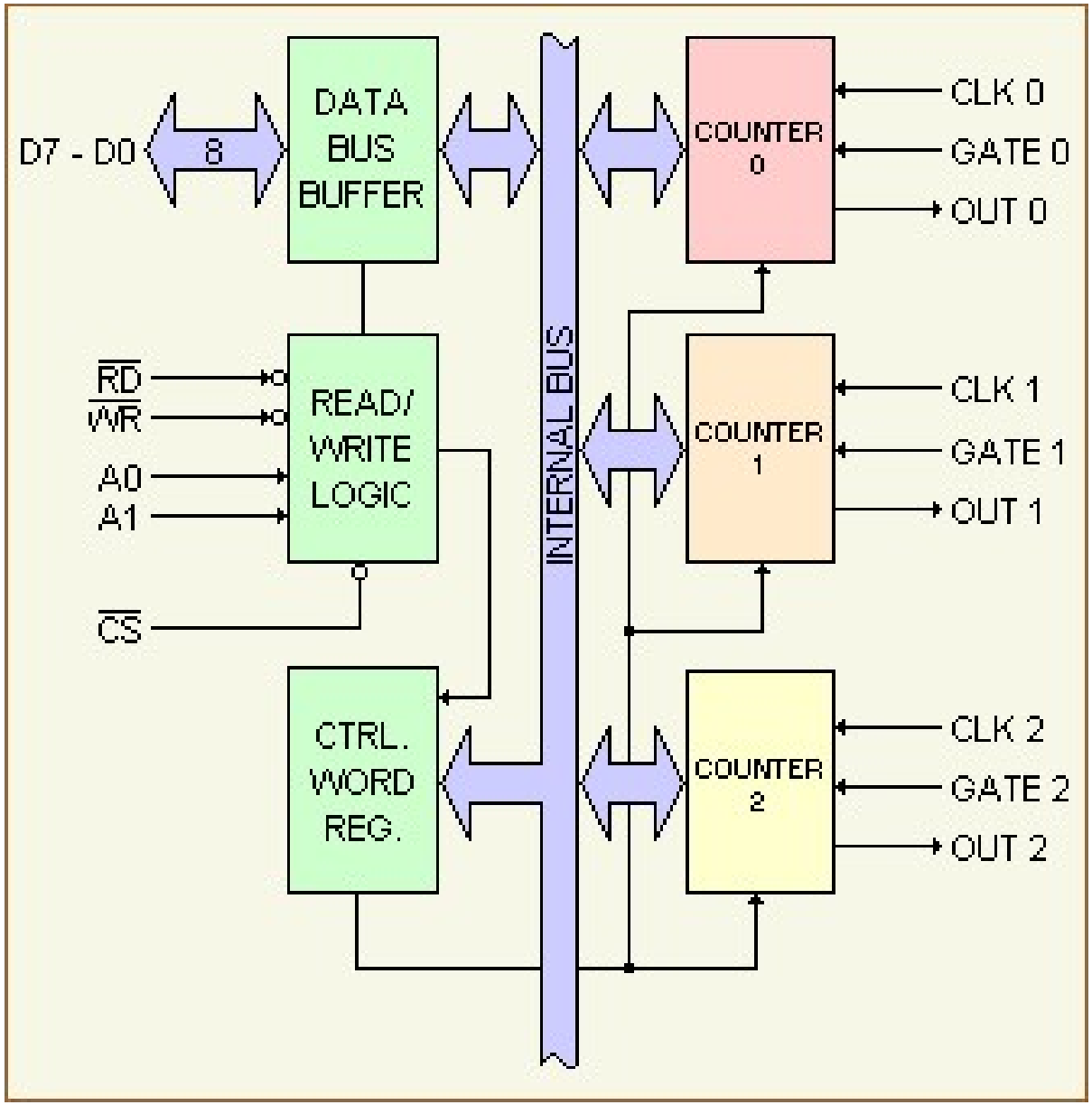
Introduction

- Facilitates the generation of accurate time delays
- So the microprocessor becomes free from the tasks related to the counting process and can execute the programs in memory.

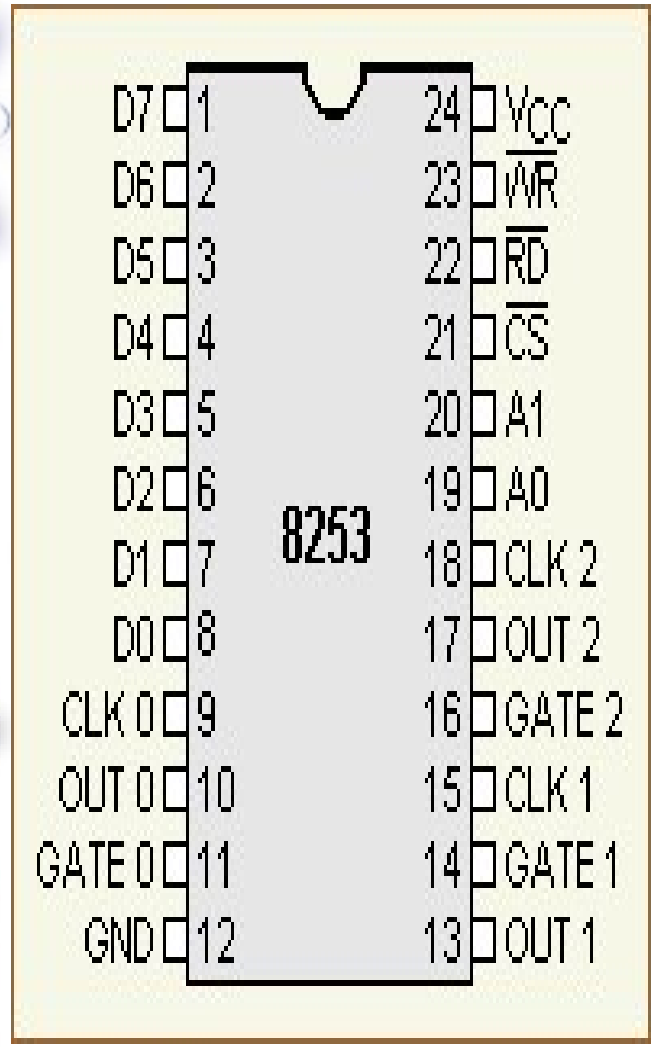
Architecture



Architecture

- 3 independent 16-bit down counters
- Operate either in BCD or in hexadecimal mode
- Each with a counter rate up to 2.6 MHz
- All the 3 counters can operate in 6 different modes
- control word register for counter setting

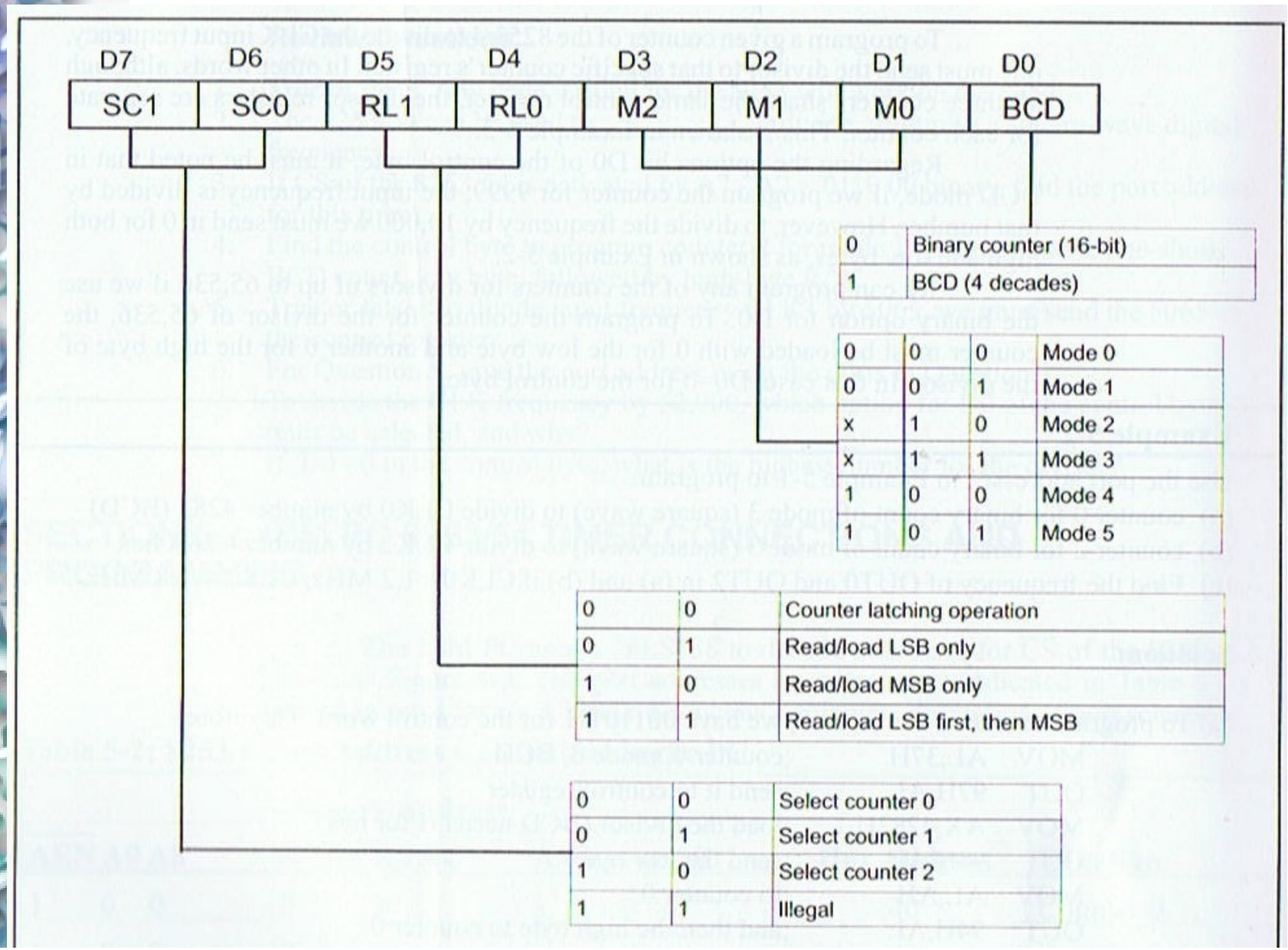
A_1	A_0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word Register



- **Out** This single output line is the signal that is the final programmed output of the device.
- **Gate** This input can act as a gate for the clock input line, or it can act as a start pulse, depending on the programmed mode of the counter.

- The specialty of the 8253 counters is that they can be easily read on line without disturbing the clock input to the counter. This facility is called as ***"on the fly reading"*** of counters, and is invoked using a mode control word.

Control Word register



mode 0: interrupt on terminal count

- The output is initially low after the mode is set. Remains same even after loading count.
- The counter start decrementing the count value after the falling edge of the clock, if the GATE input is high.
- Process continues at each falling edge

- When the terminal count is reached, the output goes high and remains high till the selected control word register or the corresponding count register is reloaded with a new mode of operation or a new count respectively .

- Writing a count register while the previous counting is in the process, generate the following sequence of response
- The first byte of the new count loaded in the count register, stop the previous count .the second byte when written, start the new count, terminating the previous count then and there .

mode 0

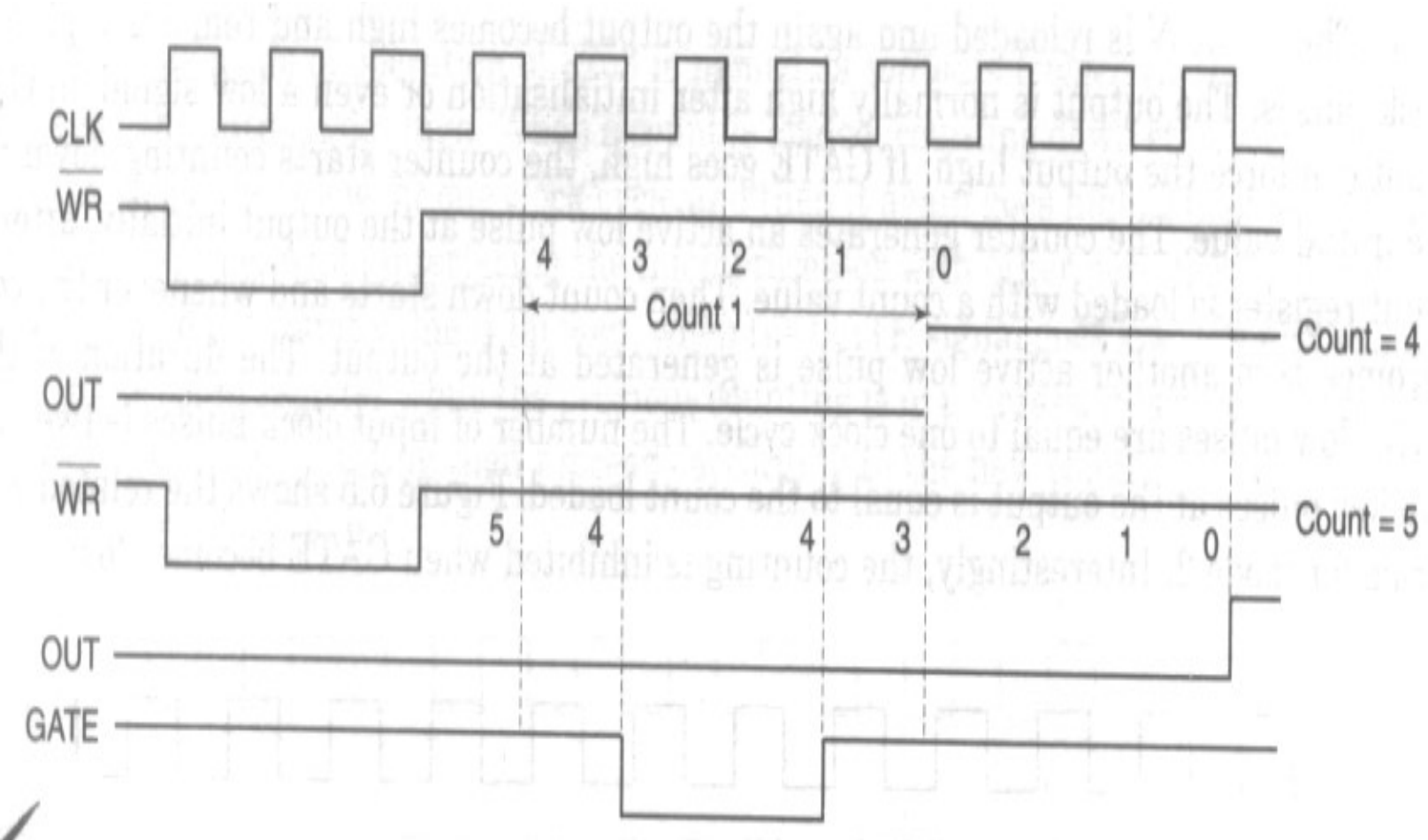


Fig. 6.3 Waveforms of $\overline{WR}$, OUT and GATE in Mode 0

mode 1: programmable one-shot

- In this mode, the 8253 can be used as a multivibrator.
- the output remains high till the suitable count is loaded in the count register and a trigger is applied through Gate.

- After the application of a trigger the output goes low and remains low till the count becomes zero.
- If another count is loaded when the output is already low, it does not disturb the previous count till a new trigger pulse is applied at a GATE input.
- The new counting starts after the new trigger pulse.

Mode 1

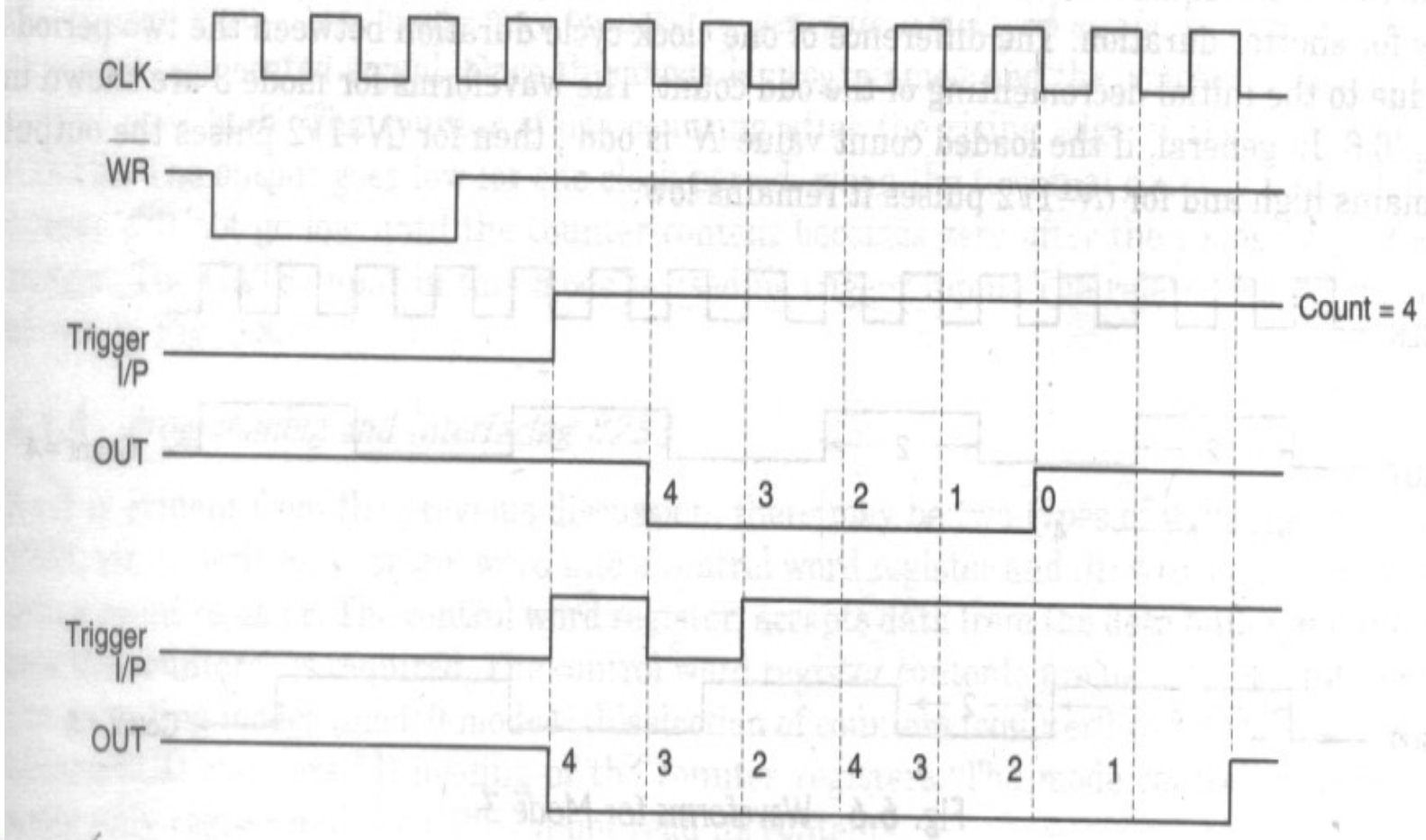


Fig. 6.4 $\overline{WR}$, GATE and OUT Waveforms for Mode 1

mode 2: rate generator

- This mode is called divides by N counter.
- if N is loaded as the count value, then, after N pulses, the output becomes low only for one clock cycle.
- The count N is reloaded and again the output become high

Mode 2

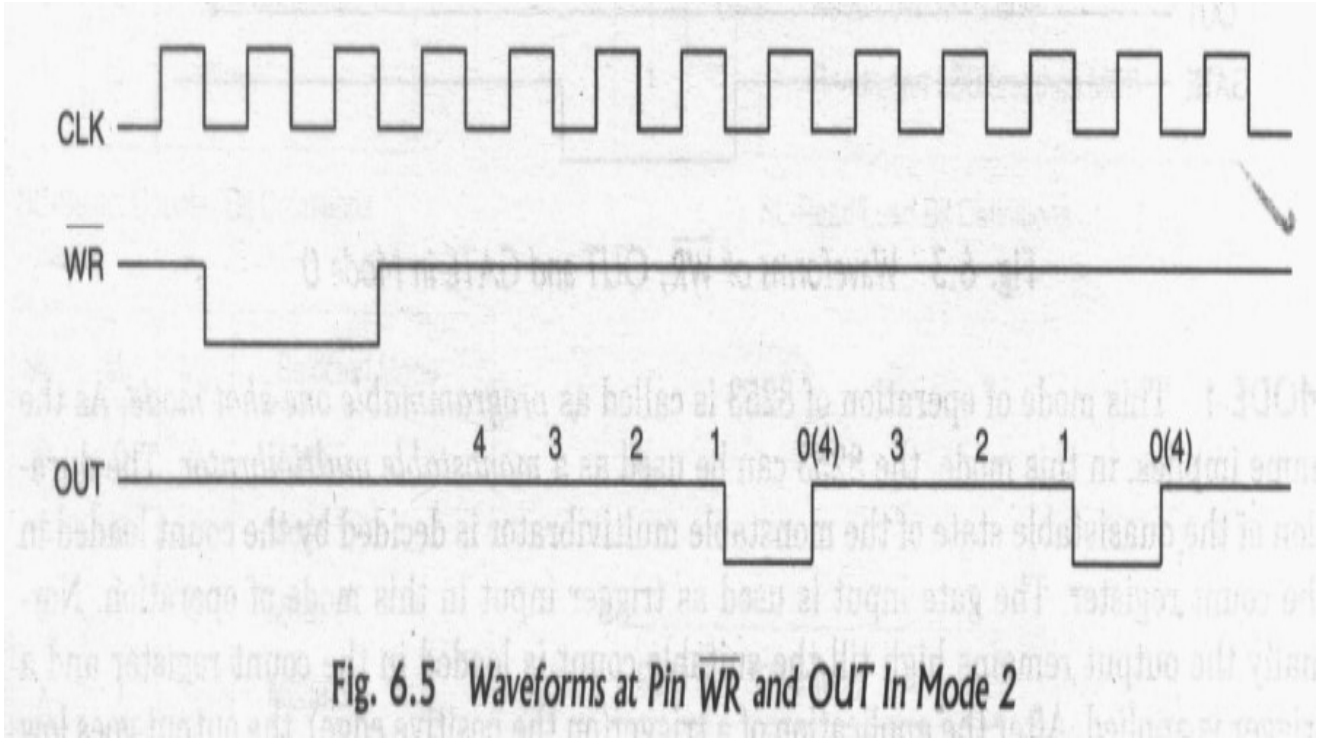


Fig. 6.5 Waveforms at Pin $\overline{WR}$ and OUT In Mode 2

mode 3: square wave generator

- When the count N loaded is even, then for half of the count, the output remains high and for the remaining half of it remaining low.
- In general the odd count value N is odd, then for (N+1)/2 pulses the output remains high and for (N-1)/2 pulses it remains low.

Mode 3

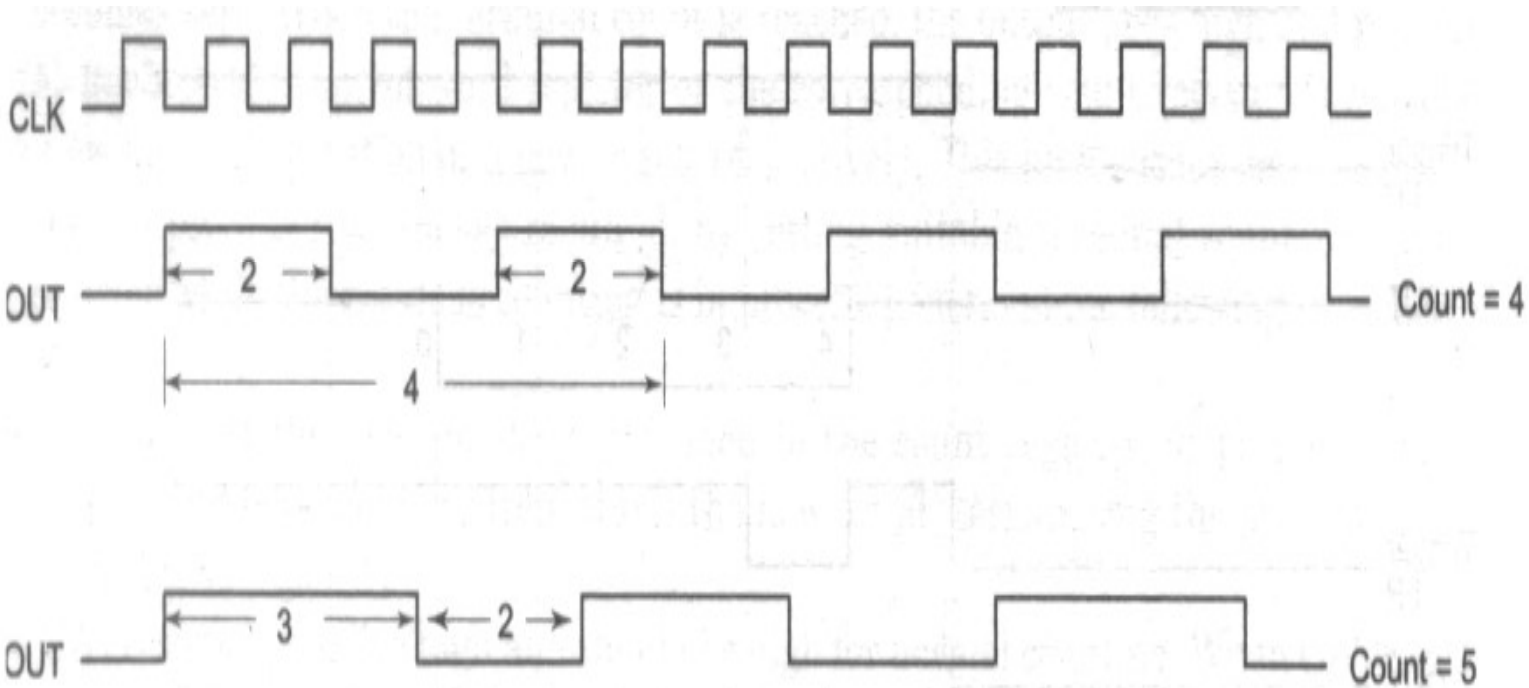


Fig. 6.6 Waveforms for Mode 3

mode 4: software triggered strobe

- After mode is set, the output goes high. When a count is loaded, counting down starts .
- On terminal count, the output goes low for one clock cycle, and then it again goes high.

- The count is inhibited and the count value is latched, when the GATE signal goes low. If a new count is loaded in the count register while the previous counting is progressed, it is accepted from the next clock cycle

Mode 4

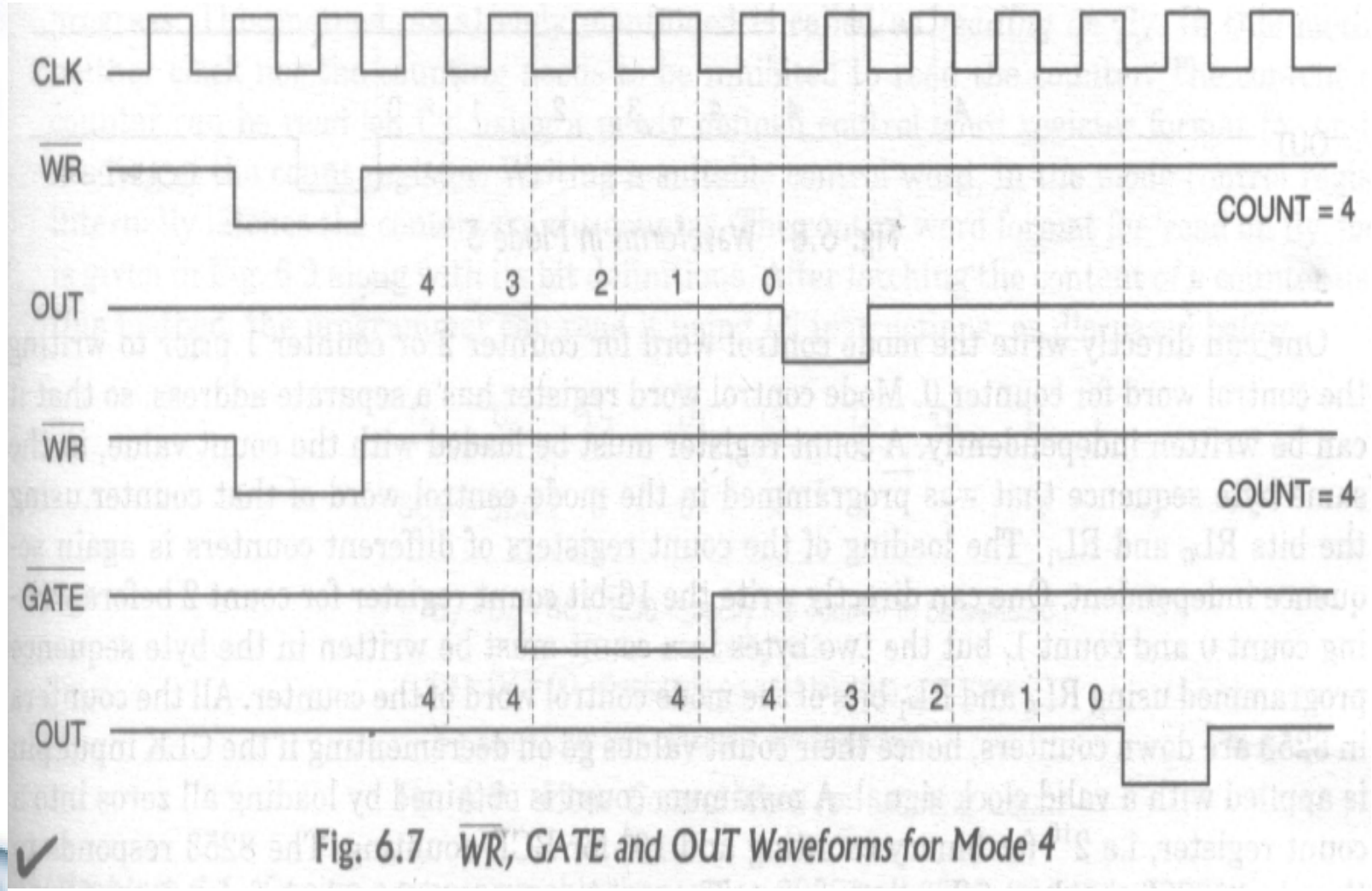


Fig. 6.7 $\overline{WR}$, GATE and OUT Waveforms for Mode 4

mode 5: hardware triggered strobe

- This mode may be used to generate a delayed strobe in response to an externally generated signal.
- Once this mode is programmed and the counter is loaded, the O/P goes high.
- The counter starts counting after the rising edge of the trigger I/P.
- The O/P goes low for one clock cycle, when the terminal count is reached.

Mode 5

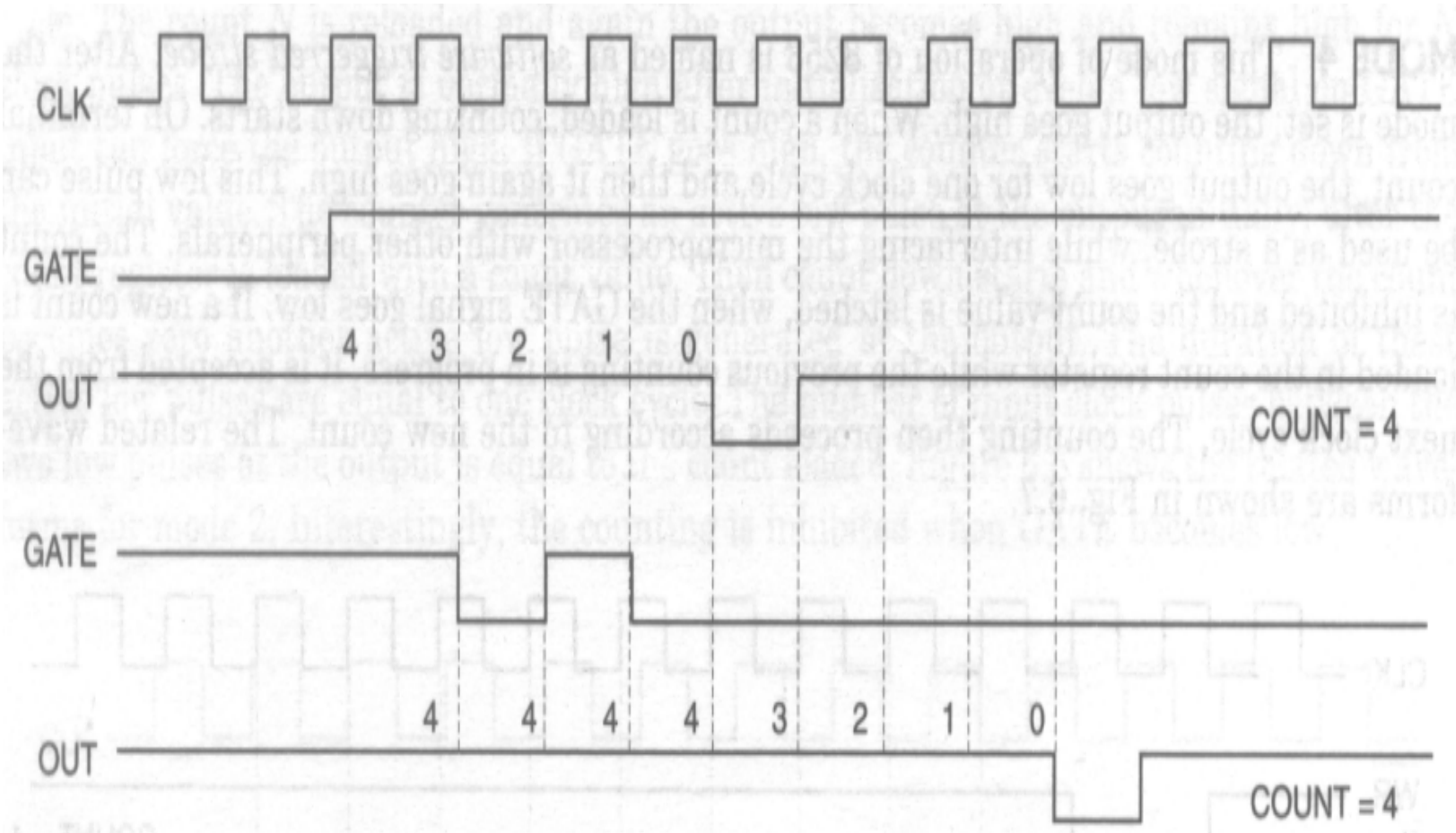


Fig. 6.8 *Waveforms in Mode 5*