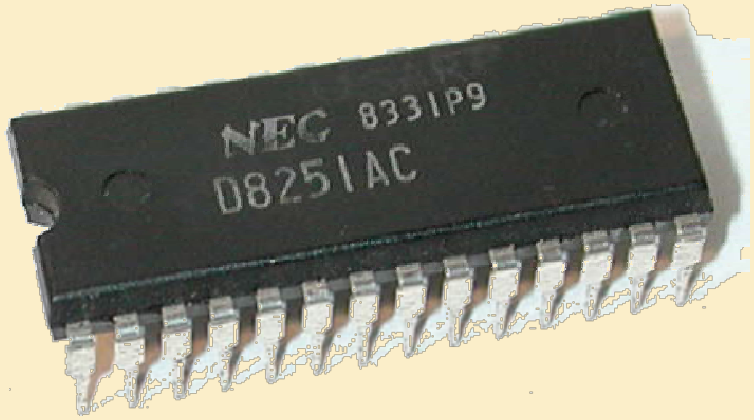
Programmable Communication Interface(USART) 8251

Universal Synchronous Asynchronous Receiver Transmitter



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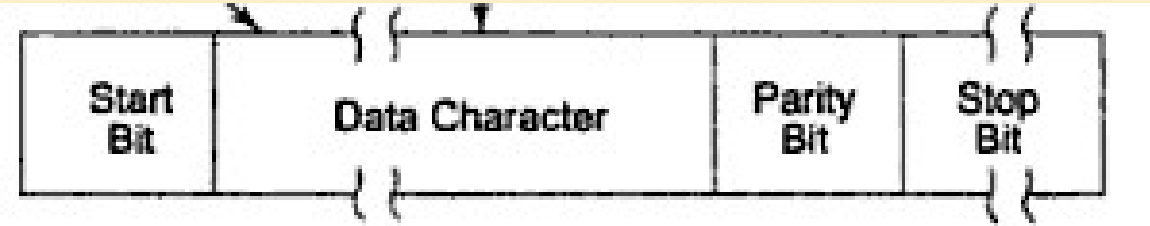
Serial Communication - Introduction

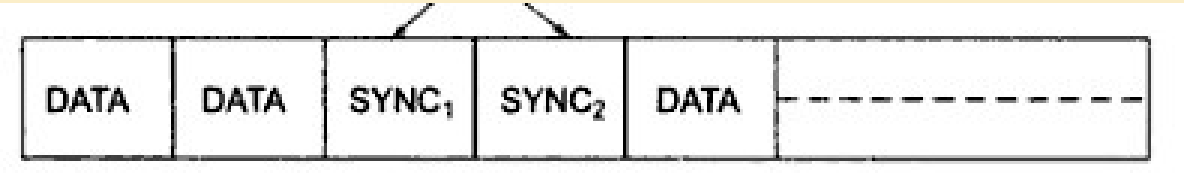
- Parallel vs Serial
- Why serial?
- Advantages & Disadvantages
- Simplex, Half-duplex, Full-duplex
- Synchronous and Asynchronous

Communication format

- Asynchronous communication format **(break characters)**



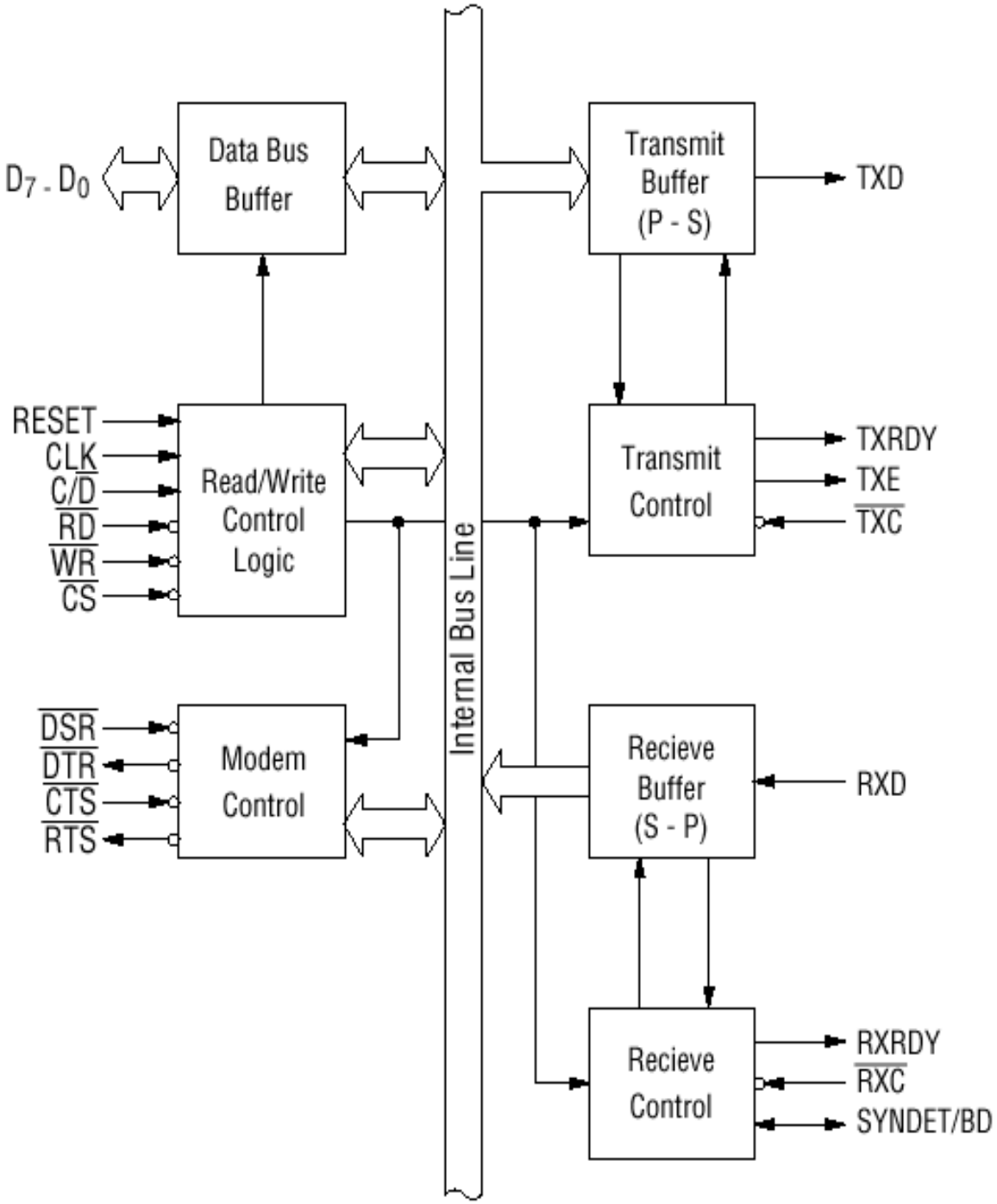
- Synchronous communication format



8251

- Function:-
  - Serial to parallel and parallel to serial conversion

Architecture - 8251



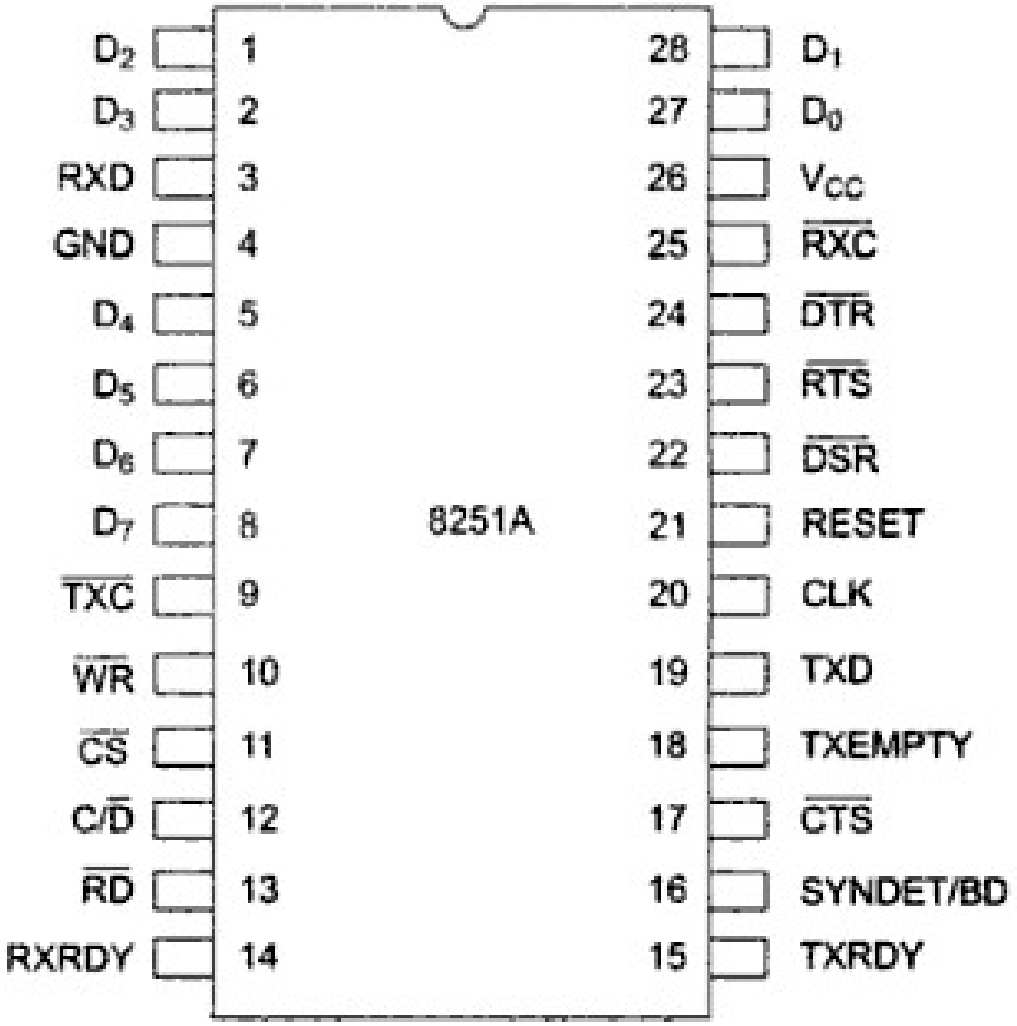


Fig. 6.27 *8251A Pin Configuration*

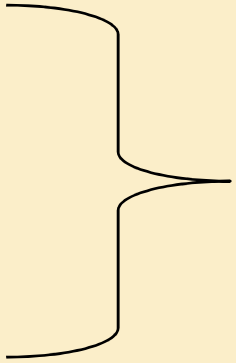
signals

- **C/D – control word or data**
  - =1 control status on the bus, =0 data on the bus
- TxC – transmitter clock input
  - Control rate at which the character is transmitted (asynchronous , synchronous)
- RxRDY
  - indicates 8251 contains character to be read by the CPU
- TxRDY
  - transmitter ready, indicates CPU that it is ready to accept new data.
- TxE – transmitter Empty
  - indicates end of transmission mode

signals

- SYNSET/BD-synch Detect/Break Detect
  - Synchronous mode:
    - o/p – indicates SYNC detect
    - i/p – will cause the IC to start assembling a data character on the rising edge of next RxC
  - Asynchronous mode:
    - Indicates break detect

- DSR – Data Set Ready
- DTR – Data Terminal Ready
- RTS – Request To Send data
- CTS – Clear To Send



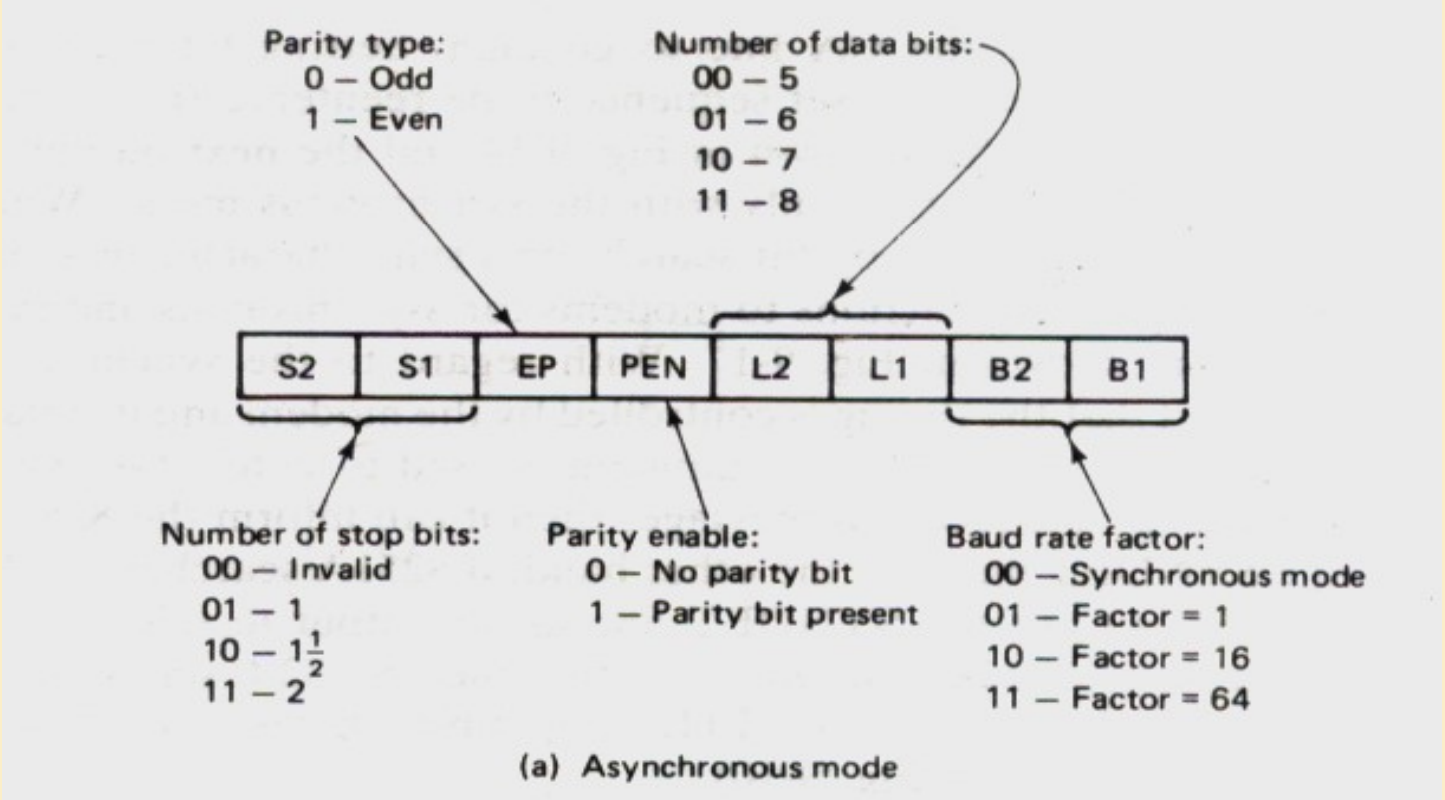
Modem signals

Initializing 8251 – control words

- Mode Instruction Control word
- Command Instruction Control word

Mode word

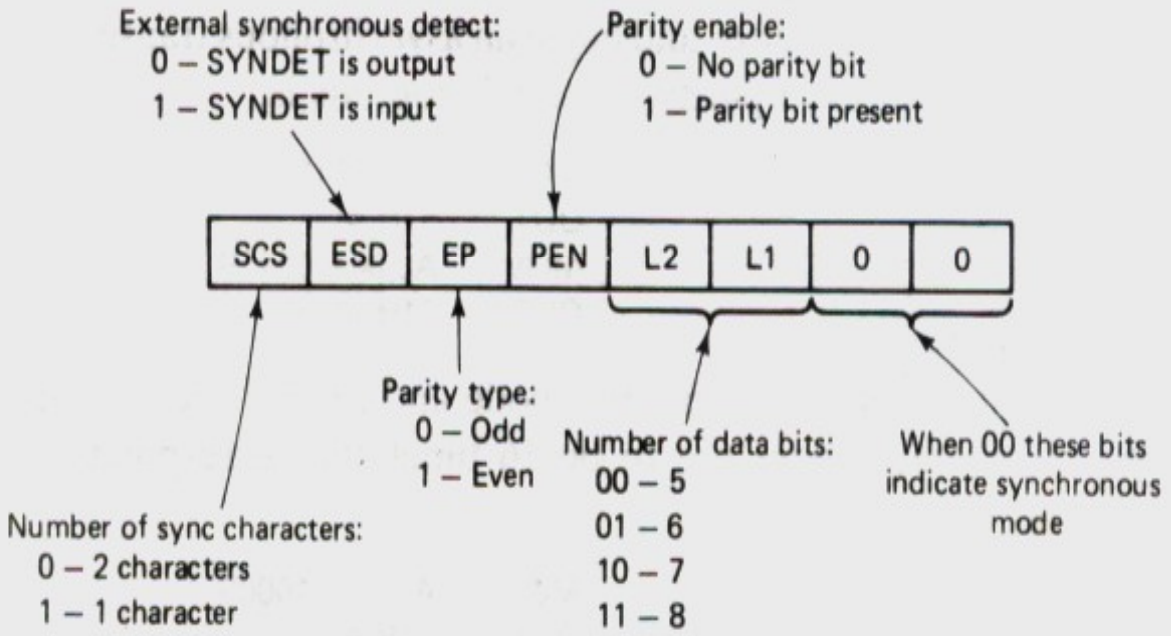
- Asynchronous mode



(a) Asynchronous mode

Mode word

- synchronous mode



(b) Synchronous mode

Figure 9-15 Format of the mode register.

Command Instruction Format

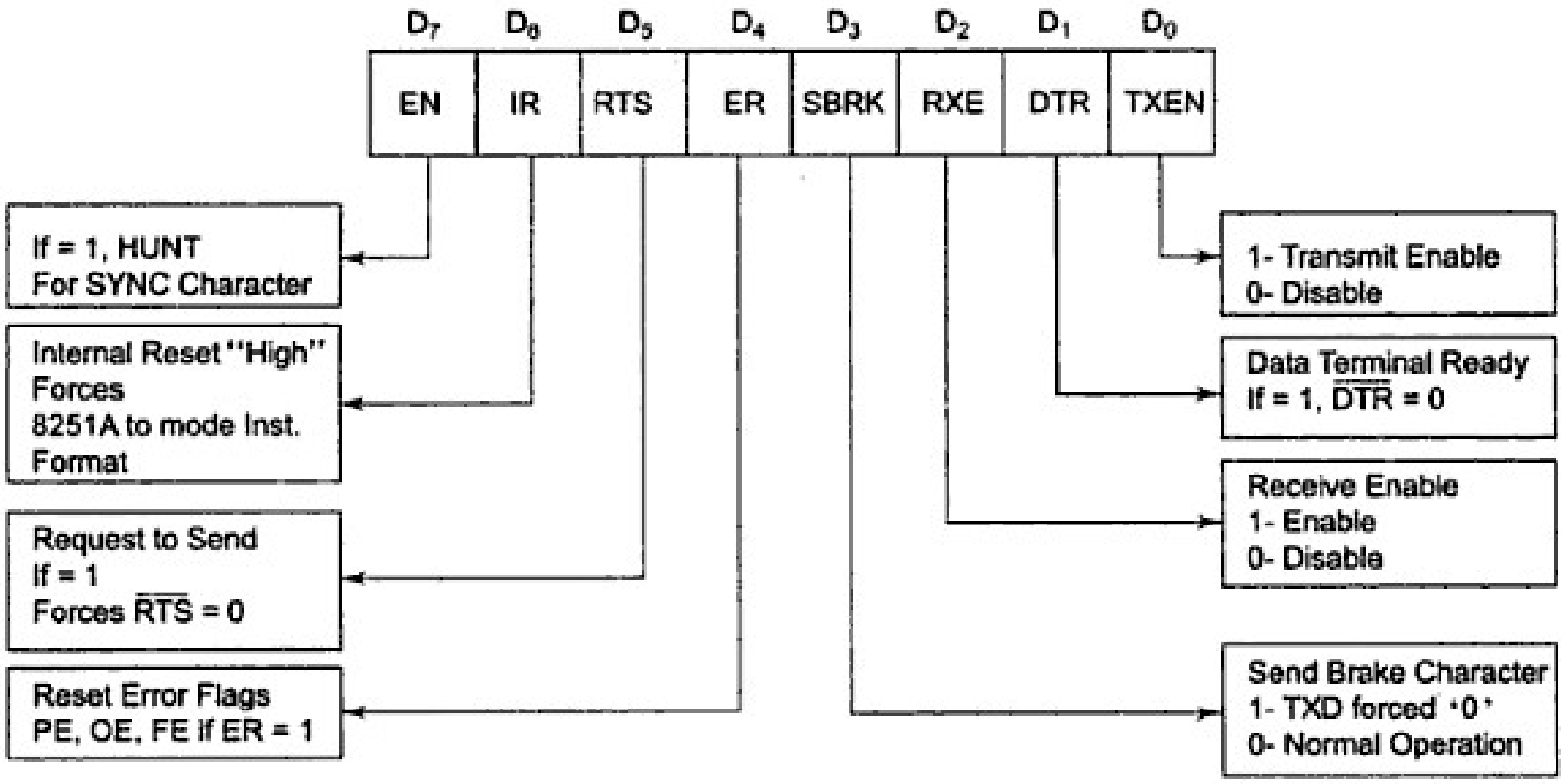


Fig. 6.33 *Command Instruction Format*

Status word

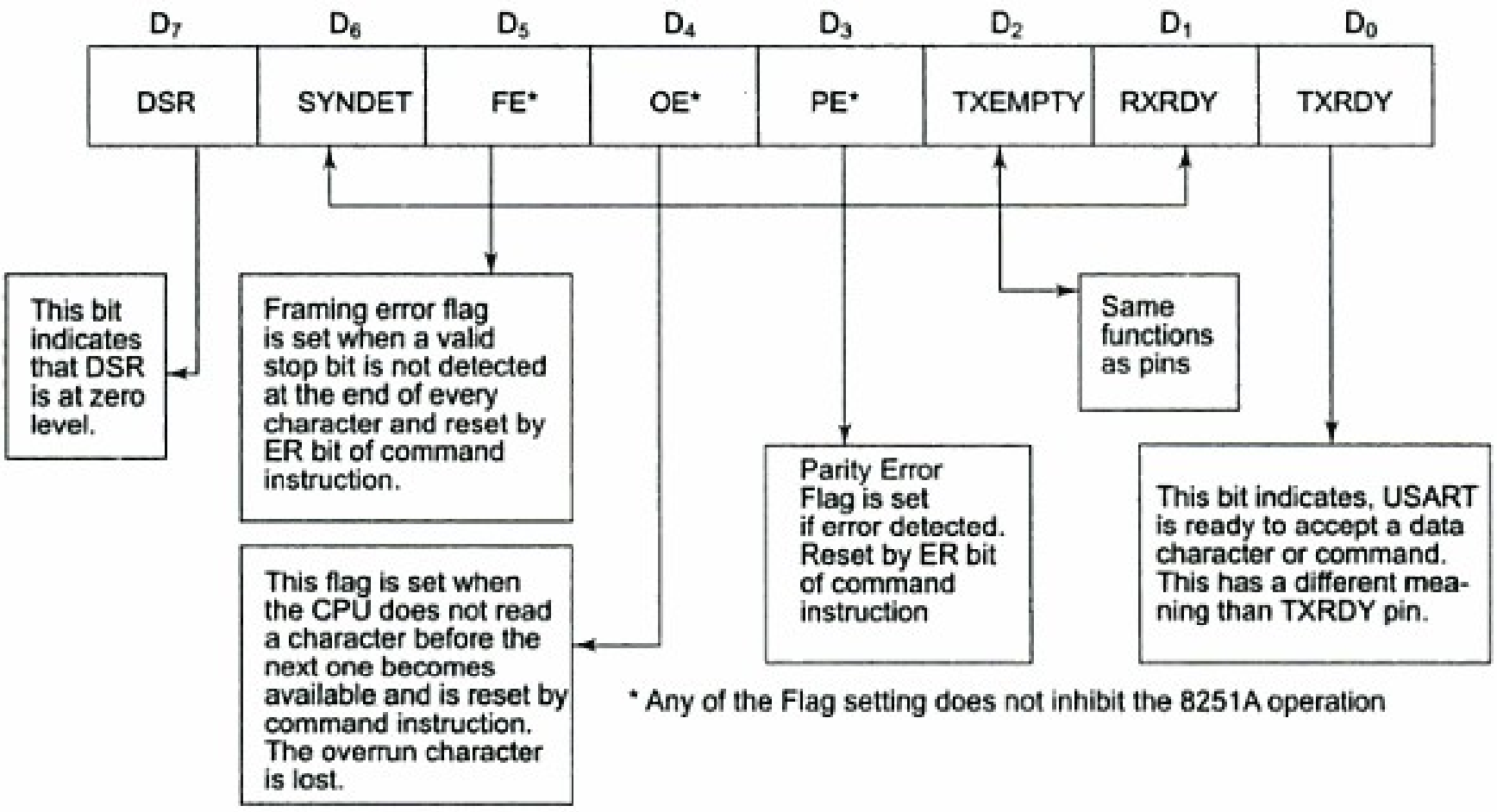


Fig. 6.34 *Status Read Instruction Format*