DMA CONTROLLER

8257

By,

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Introduction

- What is DMA?
- Event sequence
- What is 8257

Internal Architecture

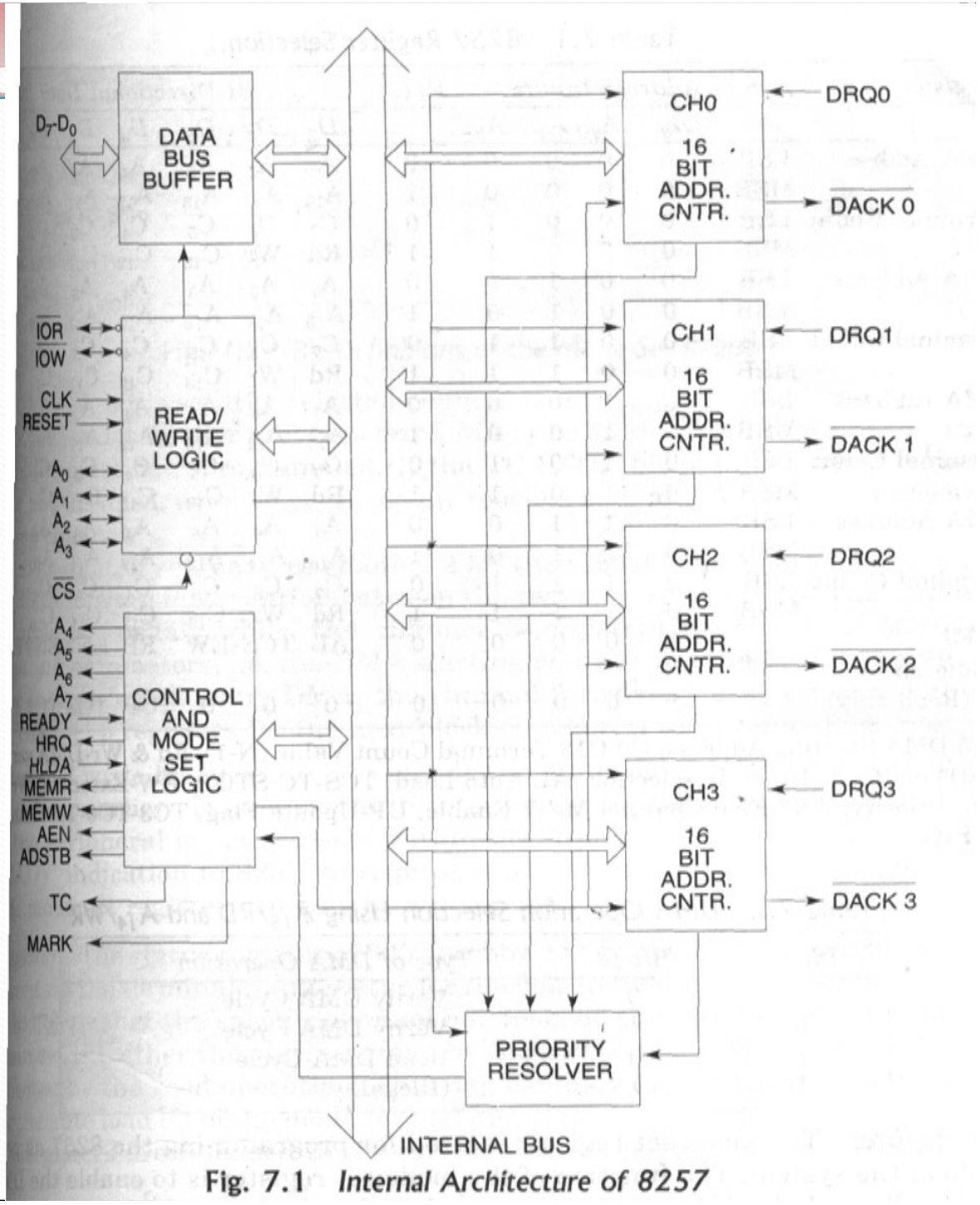


Fig. 7.1 *Internal Architecture of 8257*

- only byte by byte transfer possible
- So only 8 data lines
- Only 8 address lines, so two cycles are needed to send address

Registers

- For each Channel
  - One Address register
  - One Terminal count register
- Mode set Register
- Status register

Registers Addressed through

A0 – A3

Register	Byte	Address Inputs				F/L
		A_3	A_2	A_1	A_0	
CH-0 DMA Address	LSB	0	0	0	0	0
	MSB	0	0	0	0	1
CH-0 Terminal Count	LSB	0	0	0	1	0
	MSB	0	0	0	1	1
CH-1 DMA Address	LSB	0	0	1	0	0
	MSB	0	0	1	0	1
CH-1 Terminal Count	LSB	0	0	1	1	0
	MSB	0	0	1	1	1
CH-2 DMA Address	LSB	0	1	0	0	0
	MSB	0	1	0	0	1
CH-2 Terminal Count	LSB	0	1	0	1	0
	MSB	0	1	0	1	1
CH-3 DMA Address	LSB	0	1	1	0	0
	MSB	0	1	1	0	1
CH-3 Terminal Count	LSB	0	1	1	1	0
	MSB	0	1	1	1	1
MODE SET (Programme only)	—	1	0	0	0	0
STATUS (Read only)	—	1	0	0	0	0

Address Register(16 bit)

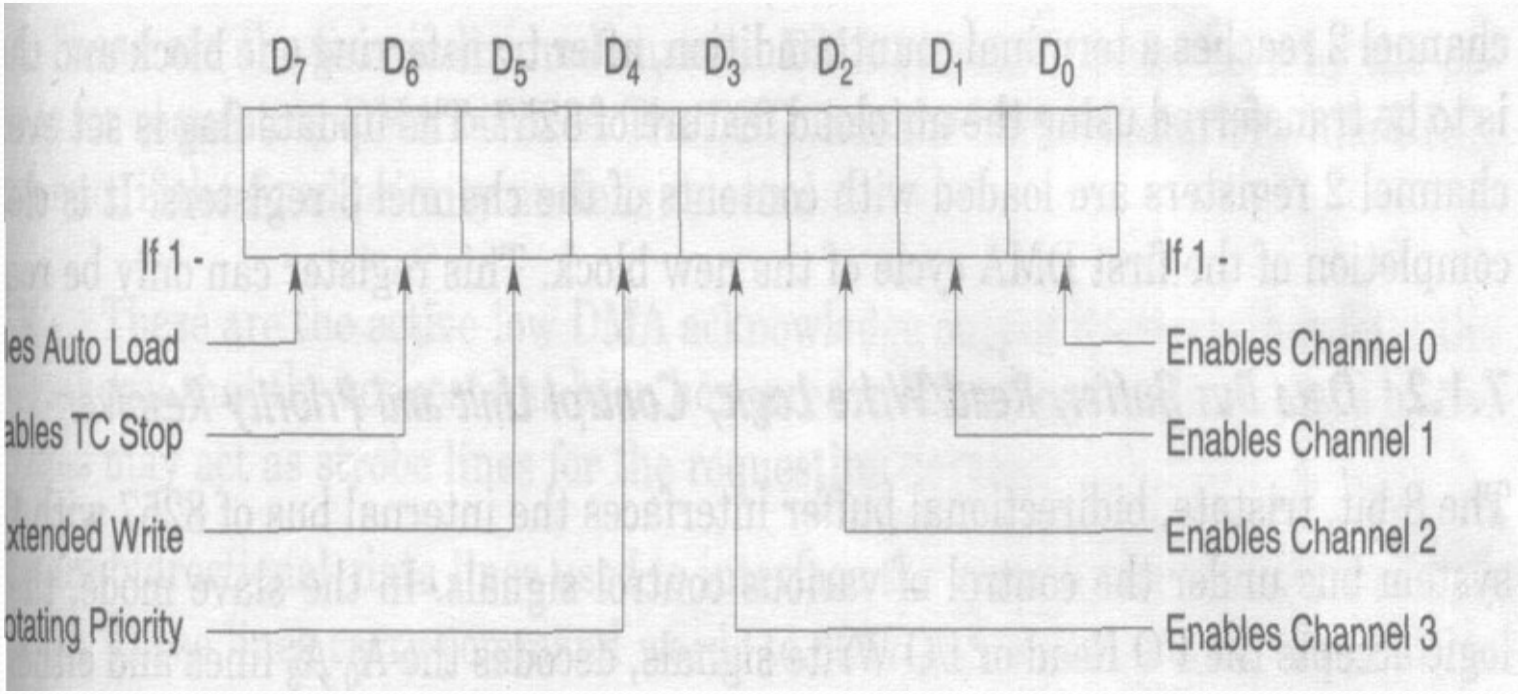
- Each DMA channel has one DMA address register.
- The function
  - To store the address of the starting memory location, which will be accessed by the DMA channel.

Terminal Count Register(16 bit)

- Each channel has one terminal count register.
- This register is used for loading the count value of DMA cycles needed.
- The low order 14 bits – count
- The bits 14 & 15 - type of DMA operation.

Bit 15	Bit 14	operation
0	0	verify
0	1	write
1	0	read
1	1	illegal

Mode set register(8 bit)



Mode set register

- Rotating priority bit

If bit D_4 is set, the rotating priority is enabled;

otherwise, the normal fixed priority is enabled.

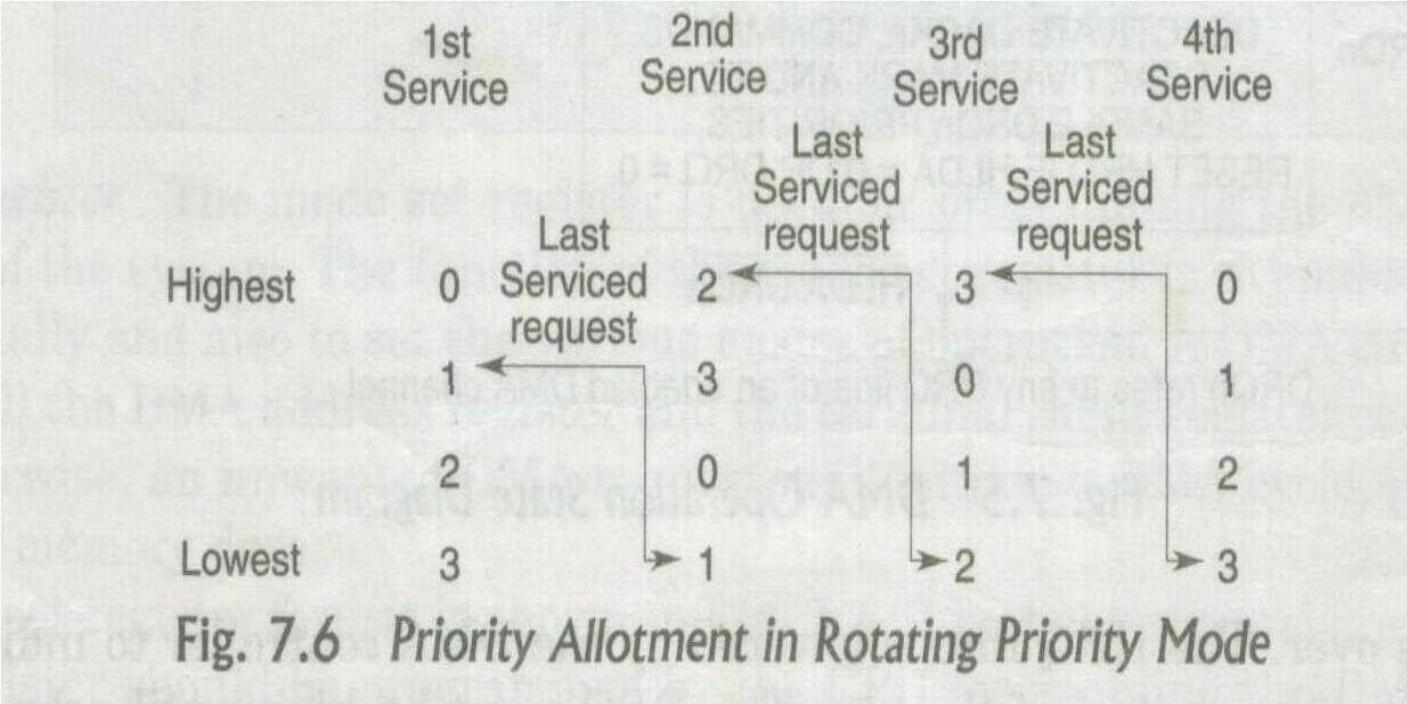


Fig. 7.6 *Priority Allotment in Rotating Priority Mode*

Mode set register

- Extended write bit : The extended write bit set, if set to '1' extends the duration of MEMW and IOW signals by activating them earlier.
- TC Stop: If the TC STOP bit is set, the selected channel is disabled after the terminal count condition is reached, and it further prevents any DMA cycle on the channel.

Mode set register

- Auto Load bit: if set, enables channel two for the repeat block chaining operation without immediate software intervention between the successive blocks.
- The channel-2 registers are used as usual, while the channel 3 registers are used to store the block re-initialization parameters, if update flag is set.

Status register (8 bit)

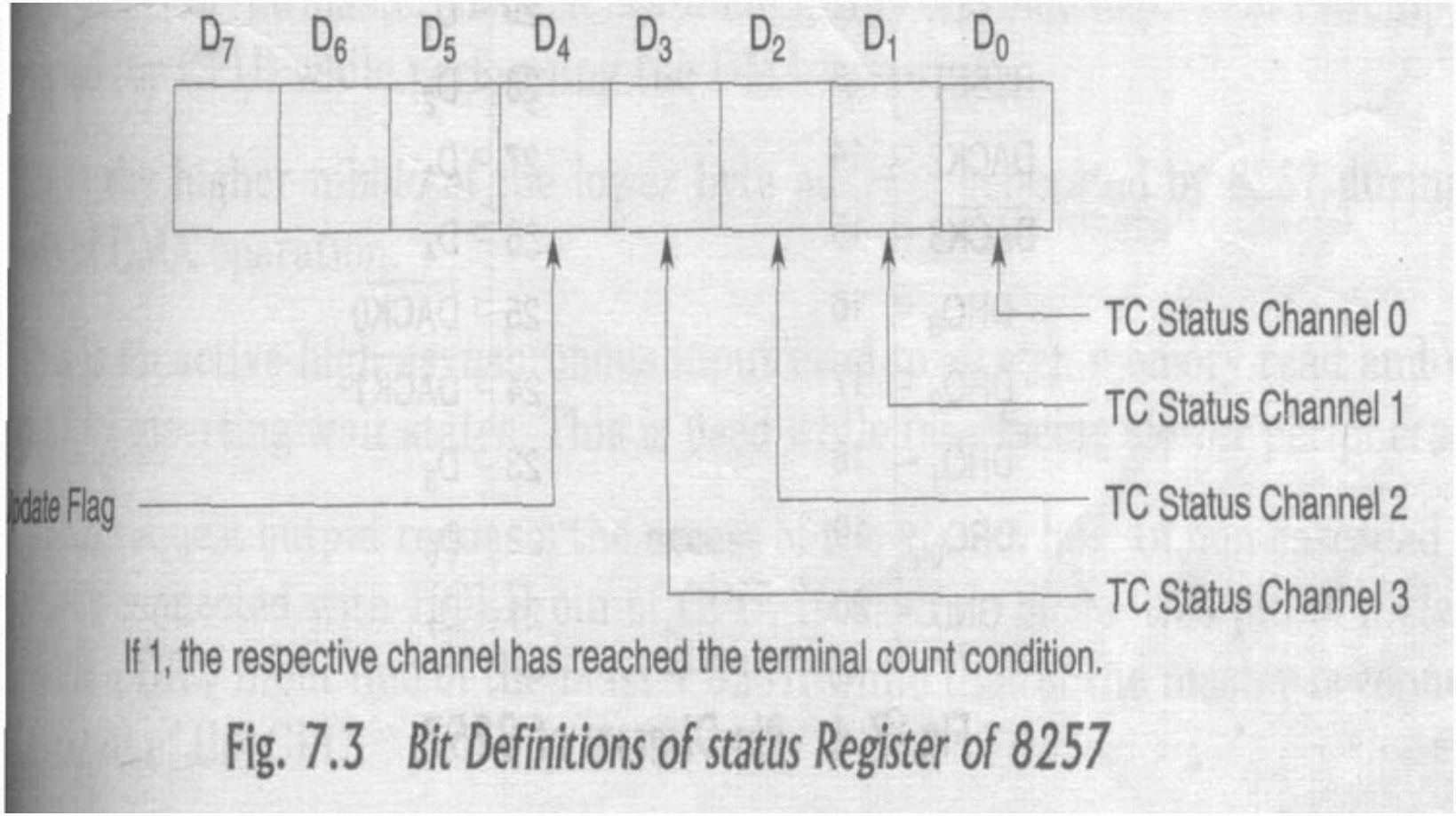


Fig. 7.3 *Bit Definitions of status Register of 8257*

Signal description 8257

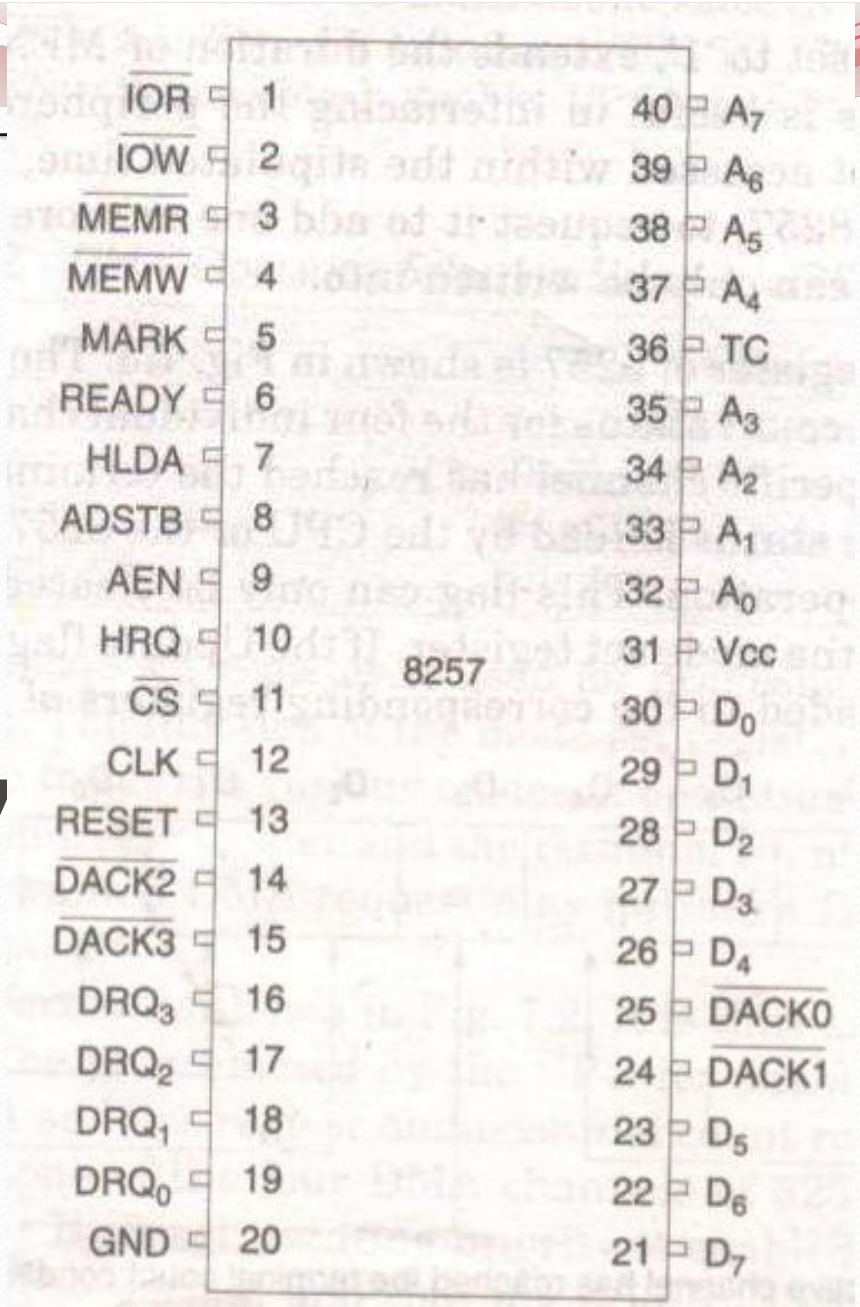


Fig. 7.4 *Pin Diagram of 8257*

DMA Transfer and operations

- A single byte transfer using 8257 may be requested by an I/O device using any one of the 8257 DRQ inputs.
- in response the 8257 sends HRQ signal to the CPU at its HOLD input and waits for acknowledgement at the HLDA input.
- If the HLDA signal is received by the DMA controller, it indicates that the bus is available for the transfer.

DMA Transfer and operations

- The DACK line of the used channel is pulled down by the DMA controller to indicate the I/O device that is request for the DMA transfer has been honored by the CPU.
- The DMA controller generates the read and write commands to transfer the byte from the I/O device.

DMA Transfer and operations

- The DACK line is pulled high after the transfer is over. To indicate the DMA controller that the transfer, as requested by the device, is over.
- The HRQ line is lowered by the DMA controller to indicate the CPU that it may regain the control of the bus. If more than one channel requests service simultaneously, the transfer will occur as a burst transfer considering priority. .

DMA Transfer and operations

- After each transfer, the 8257 checks the HLDA line. If it is found active, it completes the current transfer and releases the HRQ line and returns to its idle state.
- If the DRQ line is still active the 8257 will again activate the HRQ and proceed a s early described. It uses four clock cycles to completes a transfer.
- It has a READY input to interface it with low speed devices