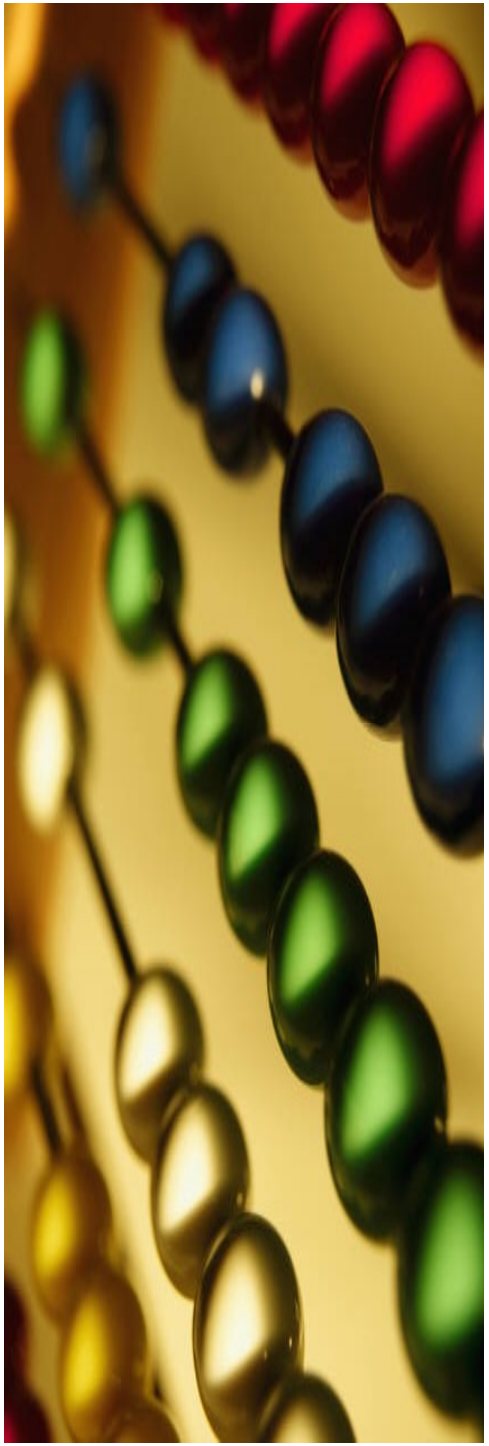

Machine Language Instructions

Addressing Modes

By,

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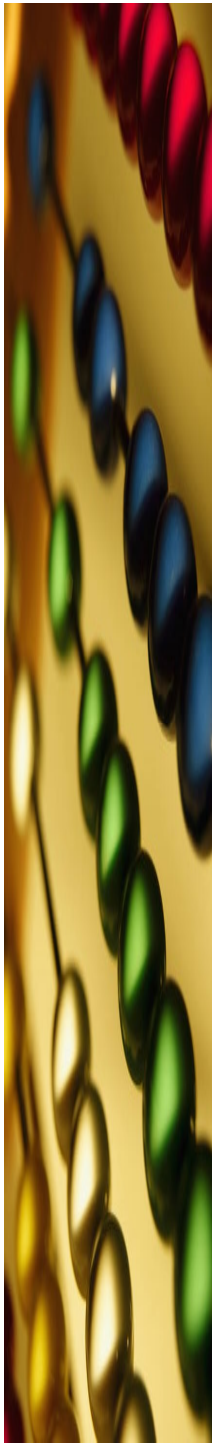
General Instruction Format

- Operation code (op code)
- Operands
- More operands – time consuming
- Limited to 2
- Extra flexible (may cause problems)

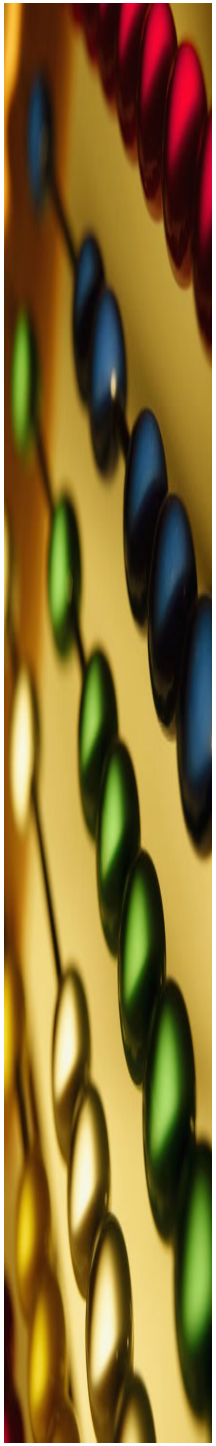
opcode	operand	operand	----	operand



Addressing modes

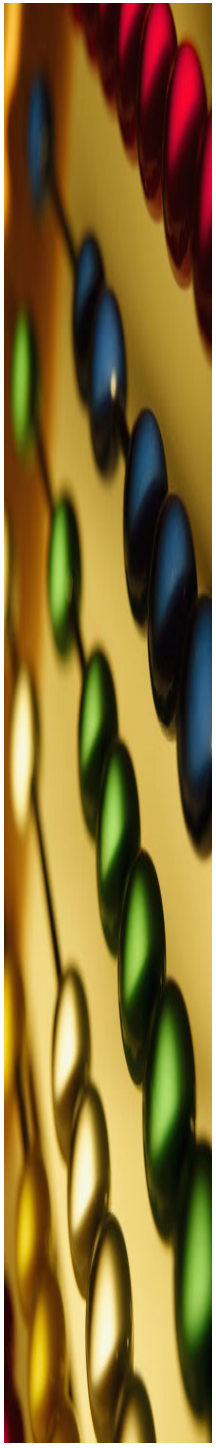
- *The way in which the operand is specified is called its addressing mode.*
- It indicates the way of locating data or operands

- Two categories
  - Those for data / sequential execution programming
  - Those for branch addresses



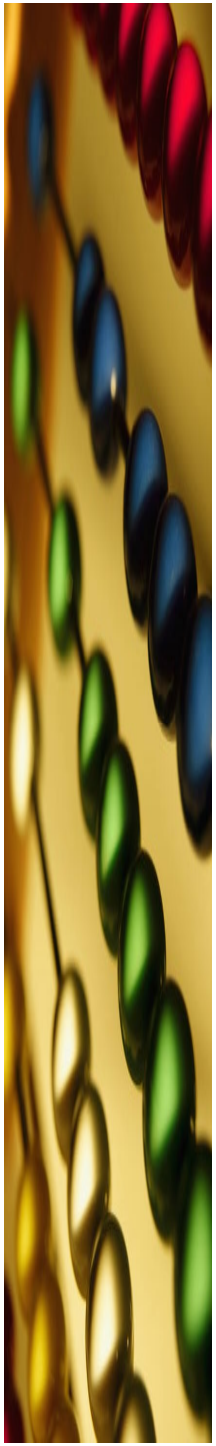
Data related addressing modes

1. Immediate – the datum is either 8 bits or 16 bits long and is part of the instruction
2. Direct – the 16 bit effective address of the datum is part of the instruction
3. Register – the datum is in the register that is specified by the instruction



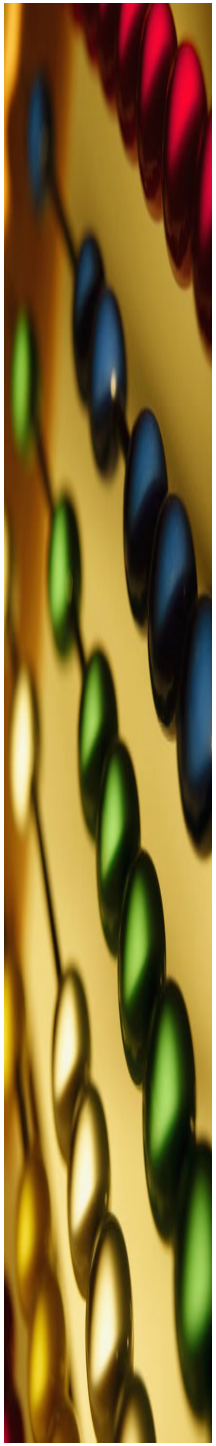
Data related addressing modes

4. Register indirect – the effective address of the datum is in the base register BX or in an index register that is specified by the instruction
5. Indexed – offset of the operand is stored in one of the index registers.
6. Register relative – the EA is the sum of an 8 bit or 16 bit displacement and the contents of a base register or an index register .



Data related addressing modes

7. Based indexed – the effective address is the sum of a base register and an index register both of which are specified by the instruction
8. Relative Based indexed – The EA is the sum of an 8 bit or 16 bit displacement and a based indexed address .



Addressing Modes

Branch Related Instructions

NEAR

Intrasegment
(CS does not change)

JUMPS and CALLS

Direct -- IP relative displacement
new IP = old IP + displacement
Short and long jumps

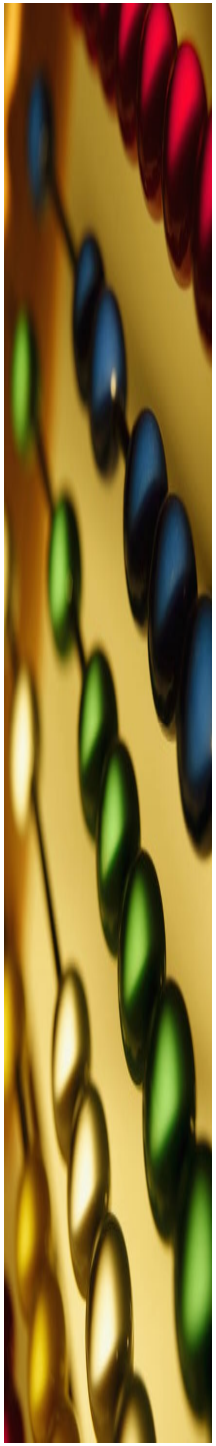
Indirect -- new IP displacement is in memory or a register.
All addressing modes apply.

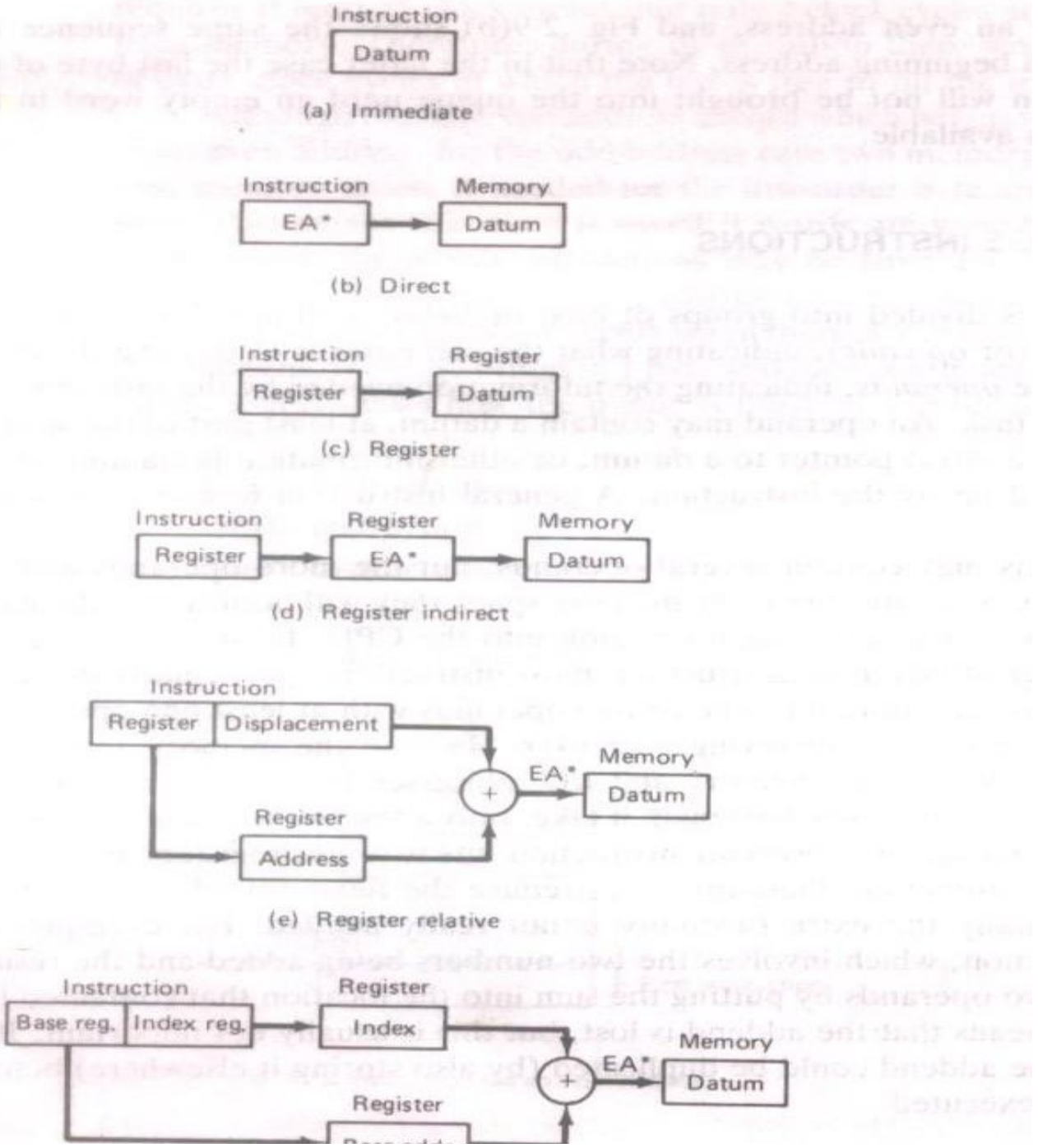
FAR

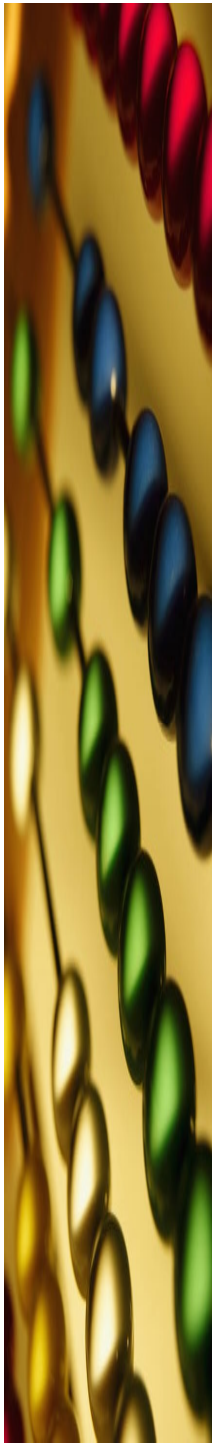
Intersegment
(CS changes)

Direct -- new CS and IP are encoded in the instruction.

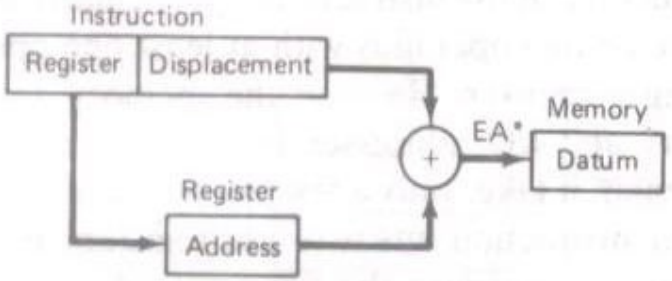
Indirect -- new CS and IP are in memory.
All addressing modes apply except immediate



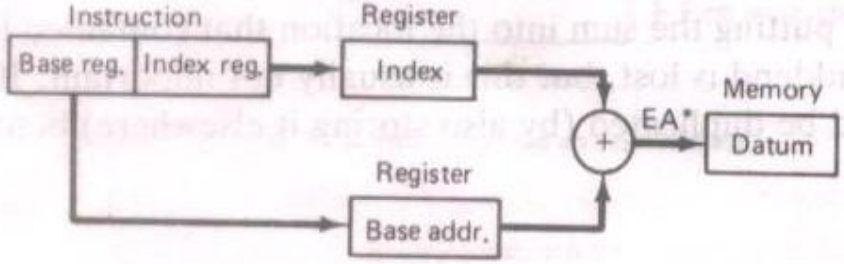

Instruction
Datum
(a) Immediate
Instruction
Memory
EA*
Datum
(b) Direct
Instruction
Register
Register
Datum
(c) Register
Instruction
Register
Memory
Register
EA*
Datum
(d) Register indirect
Instruction
Register
Displacement
Memory
EA*
+
Datum
Register
Address
(e) Register relative
Instruction
Register
Base reg.
Index reg.
Index
Memory
EA*
+
Datum
Register



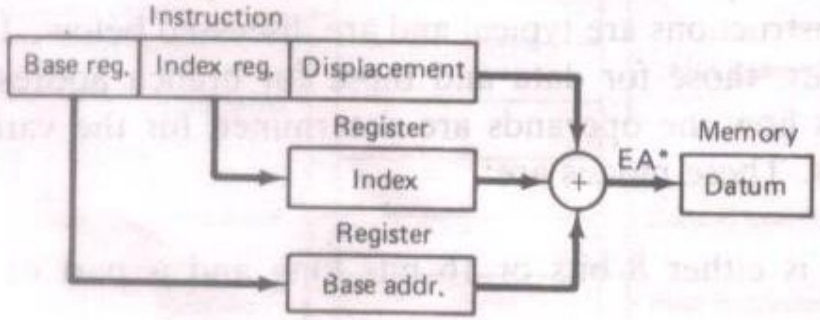
(d) Register indirect



(e) Register relative



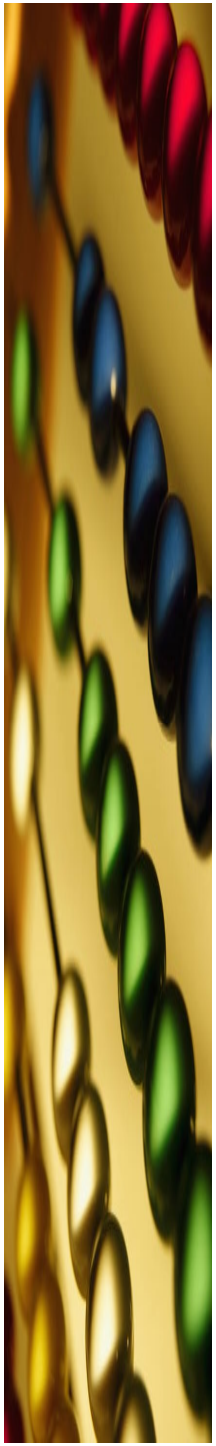
(f) Based indexed

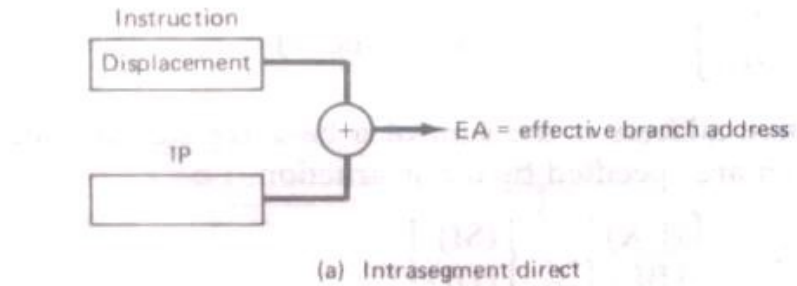


(g) Relative based indexed

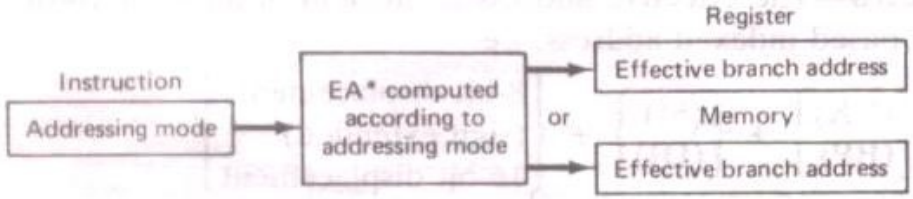
*EA is added to 16_{10} times the contents of the appropriate segment register.

Figure 2-11 modes.

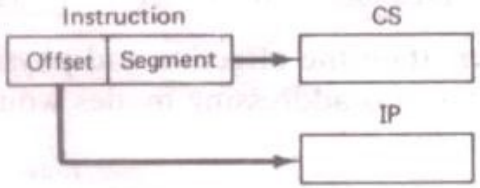




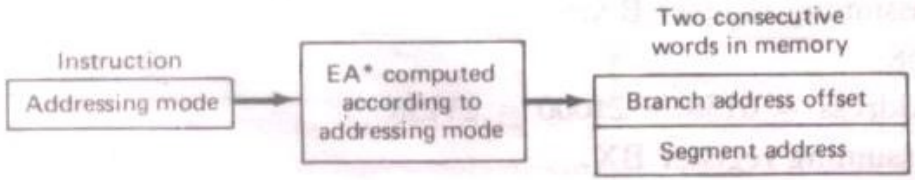
(a) Intrasegment direct



(b) Intrasegment indirect



(c) Intersegment direct



(d) Intersegment indirect

*EA is added to 16_{10} times the contents of the appropriate segment register.

Figure 2· modes.