Minimum and Maximum Mode

System and Timings

By,

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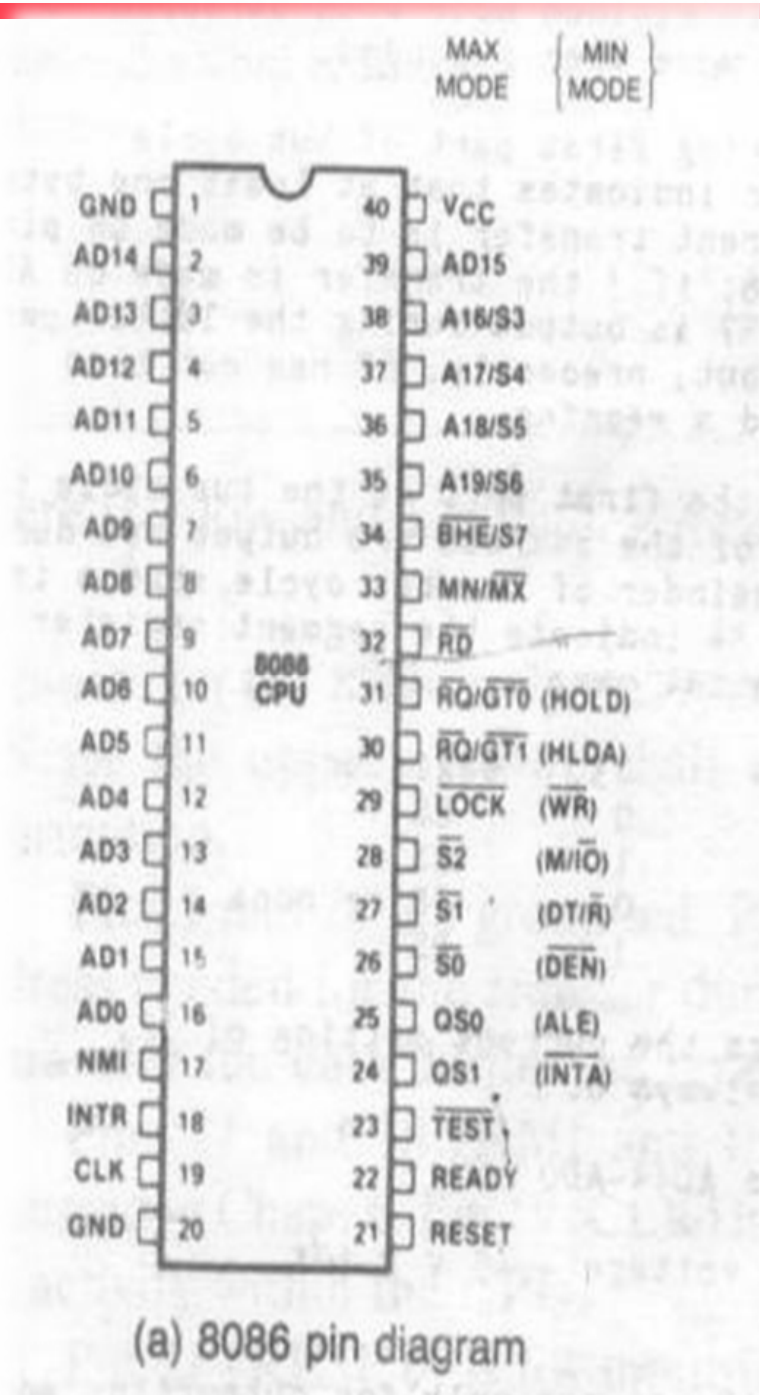
- **Pin 33 (MN/$\overline{\text{MX}}$)**
- Minimum mode

  used for small system with a single processor
- Maximum mode

  used for medium system to large system includes two or more processors.



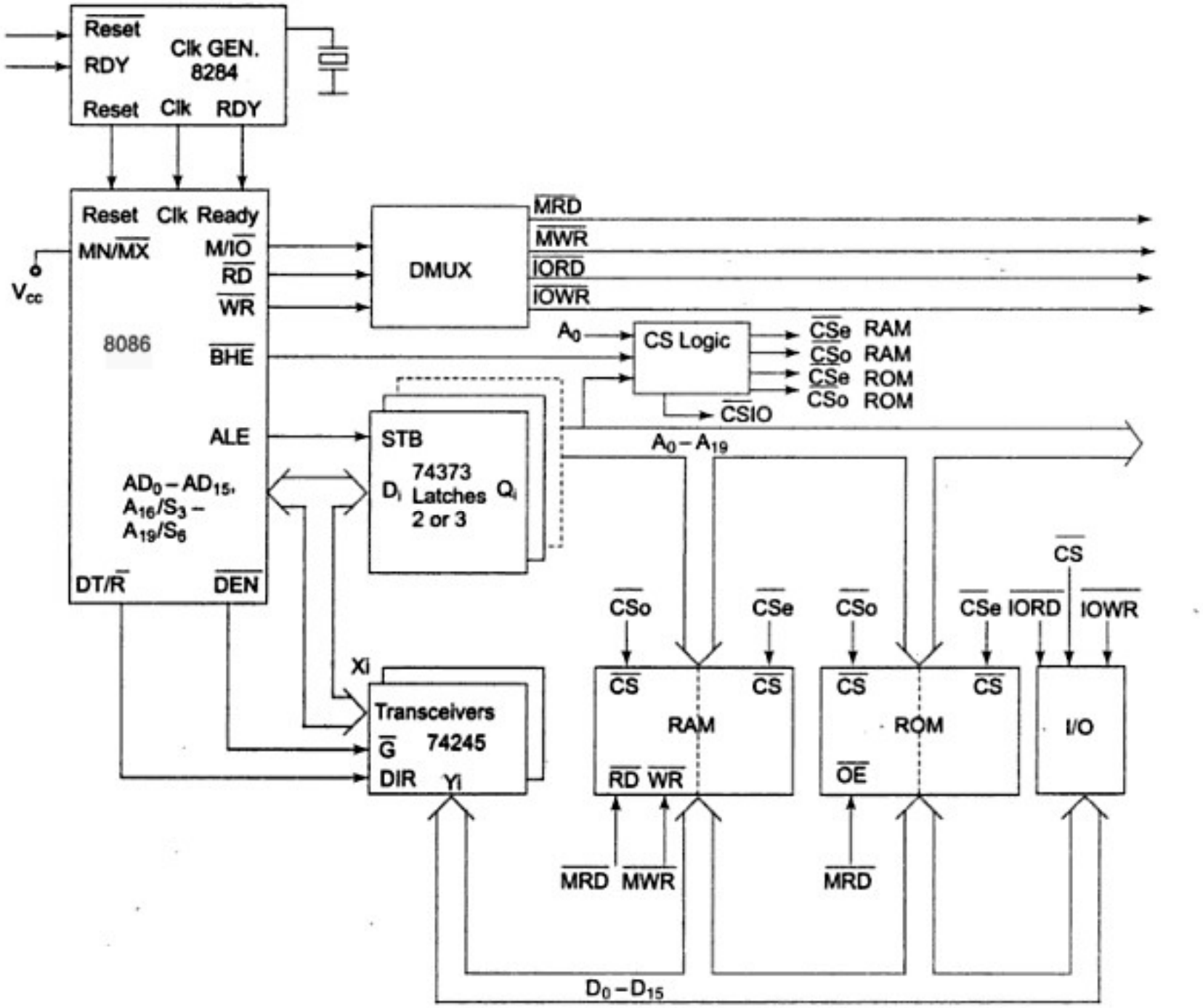
(a) 8086 pin diagram

MINIMUM MODE

Minimum Mode Pins

Pin	Symbol	In/Out 3-State	Description
24	$\overline{INTA}$	O-3	Indicates recognition of an interrupt request. Consists of two negative going pulses in two consecutive bus cycles.
25	ALE	O	Outputs a pulse at the beginning of the bus cycle and is to indicate an address is available on the address pins.
26	$\overline{DEN}$	O-3	Output during the latter portion of the bus cycle and is to inform the transceivers that the CPU is ready to send or receive data.
27	DT/$\overline{R}$	O-3	Indicates to the set of transceivers whether they are to transmit (1) or receive (0) data.
28[1]	M/$\overline{IO}$	O-3	Distinguishes a memory transfer from an I/O transfer. For a memory transfer it is 1.
29	$\overline{WR}$	O-3	When 0, it indicates a write operation is being performed. It is used in conjunction with pins 28 (M/$\overline{IO}$) and 32 ($\overline{RD}$) to specify the type of transfer.
30	HLDA	O	Outputs a bus grant to a requesting master. Pins with tristate gates are put in high impedance state while HLDA=1.
31	HOLD	I	Receives bus requests from bus masters. The 8086/8088 will not gain control of the bus until this signal is dropped.

[1]For the 8088, the symbol is IO/$\overline{M}$ and a 1 indicates an I/O transfer.


Reset
RDY
Clk GEN.
8284
Reset Clk RDY
Reset Clk Ready
MN/MX
M/IO
RD
WR
BHE
ALE
AD0 – AD15,
A16/S3 –
A19/S6
DT/R
DEN
8086
Vcc
DMUX
MRD
MWR
IORD
IOWR
A0
CS Logic
CSe RAM
CSo RAM
CSe ROM
CSo ROM
CSIO
A0 – A19
STB
74373
Di Latches Qi
2 or 3
Xi
Transceivers
G 74245
DIR Yi
CSo
CSe
CSo
CSe IORD
IOWR
CS
CS CS
RAM
RD WR
CS CS
ROM
OE
I/O
MRD MWR
MRD
D0 – D15

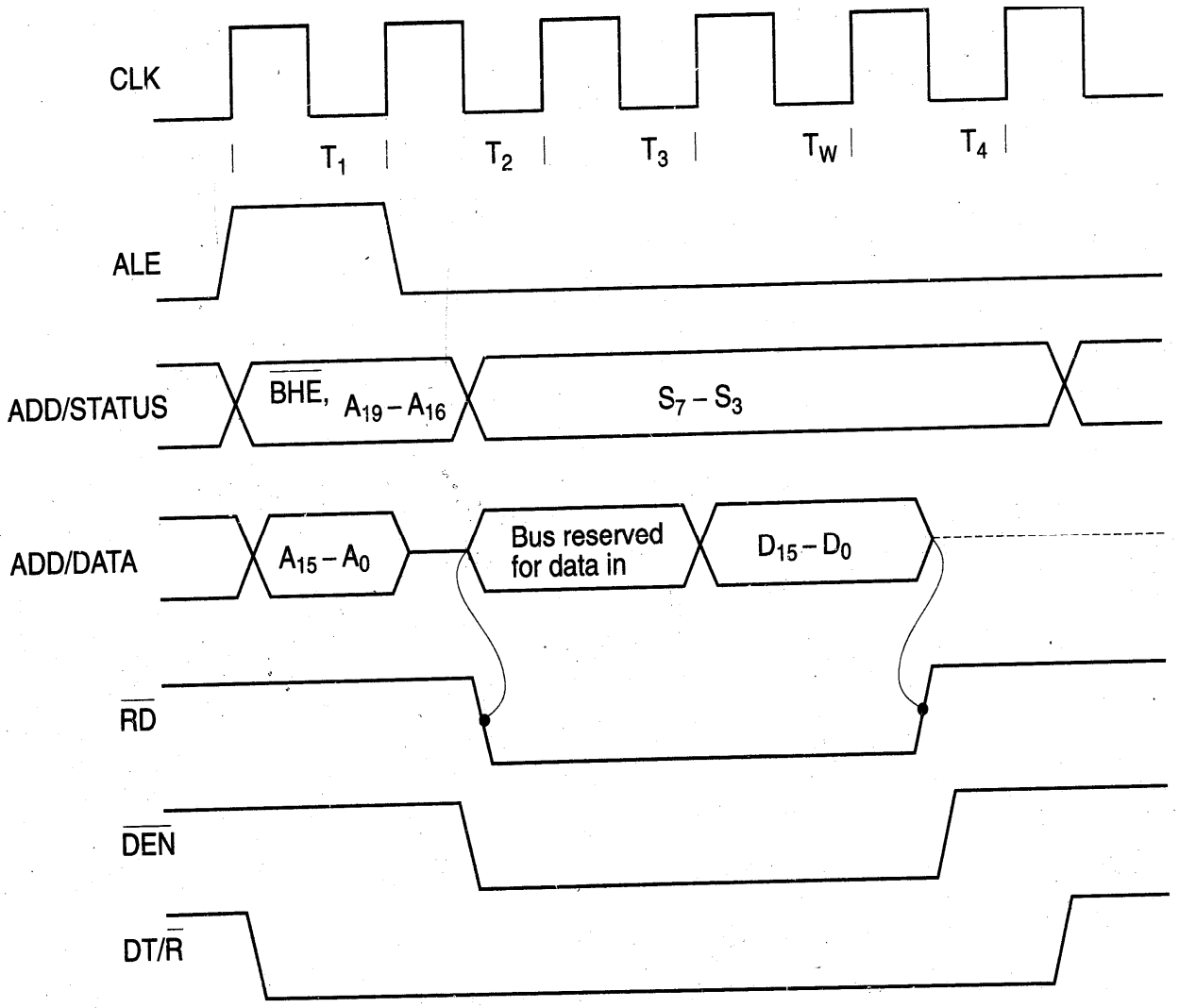


Fig.1.9(a) *Read Cycle Timing Diagram for Minimum Mode*

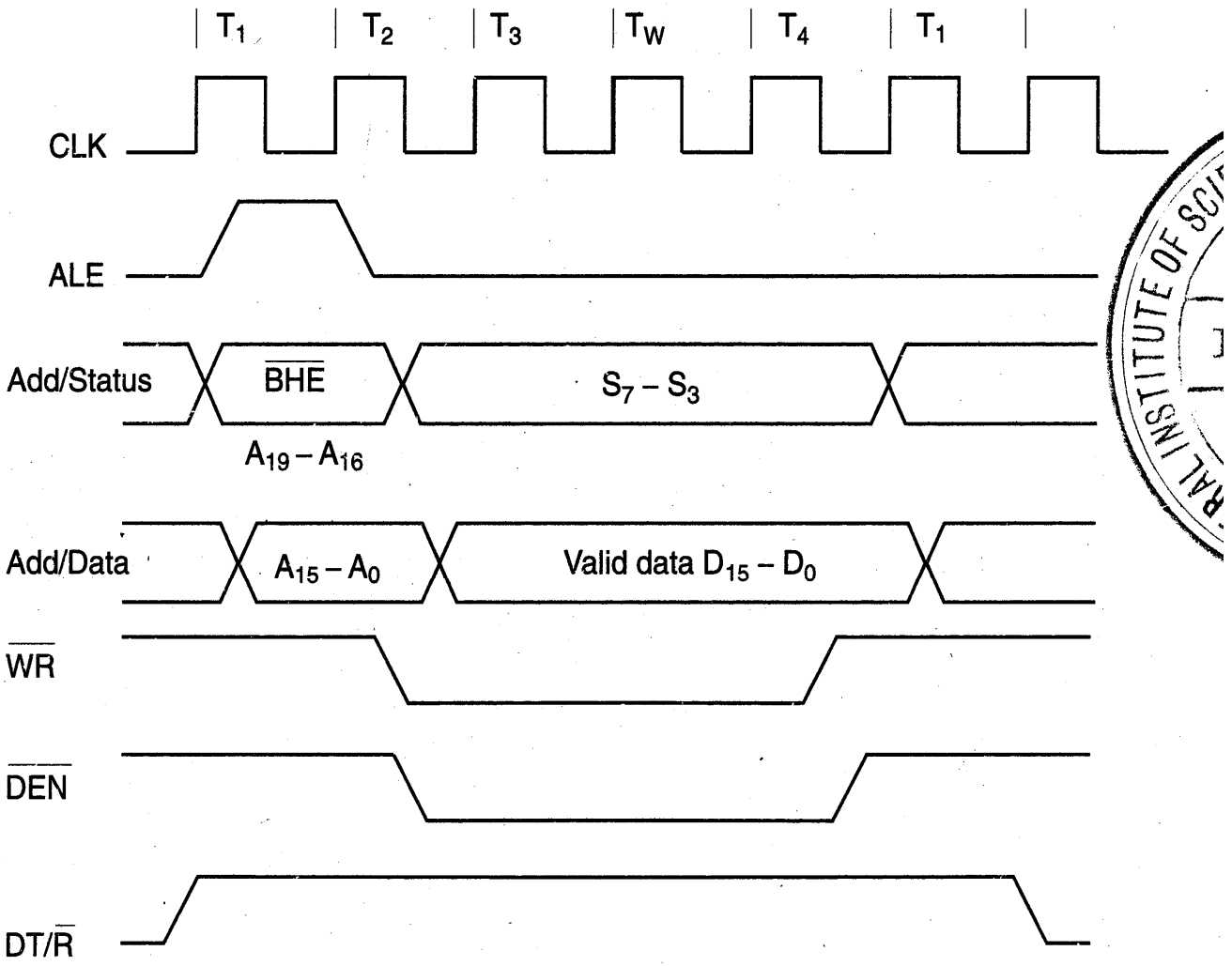


Fig.1.9(b) *Write Cycle Timing Diagram for Minimum Operation*

MAXIMUM MODE

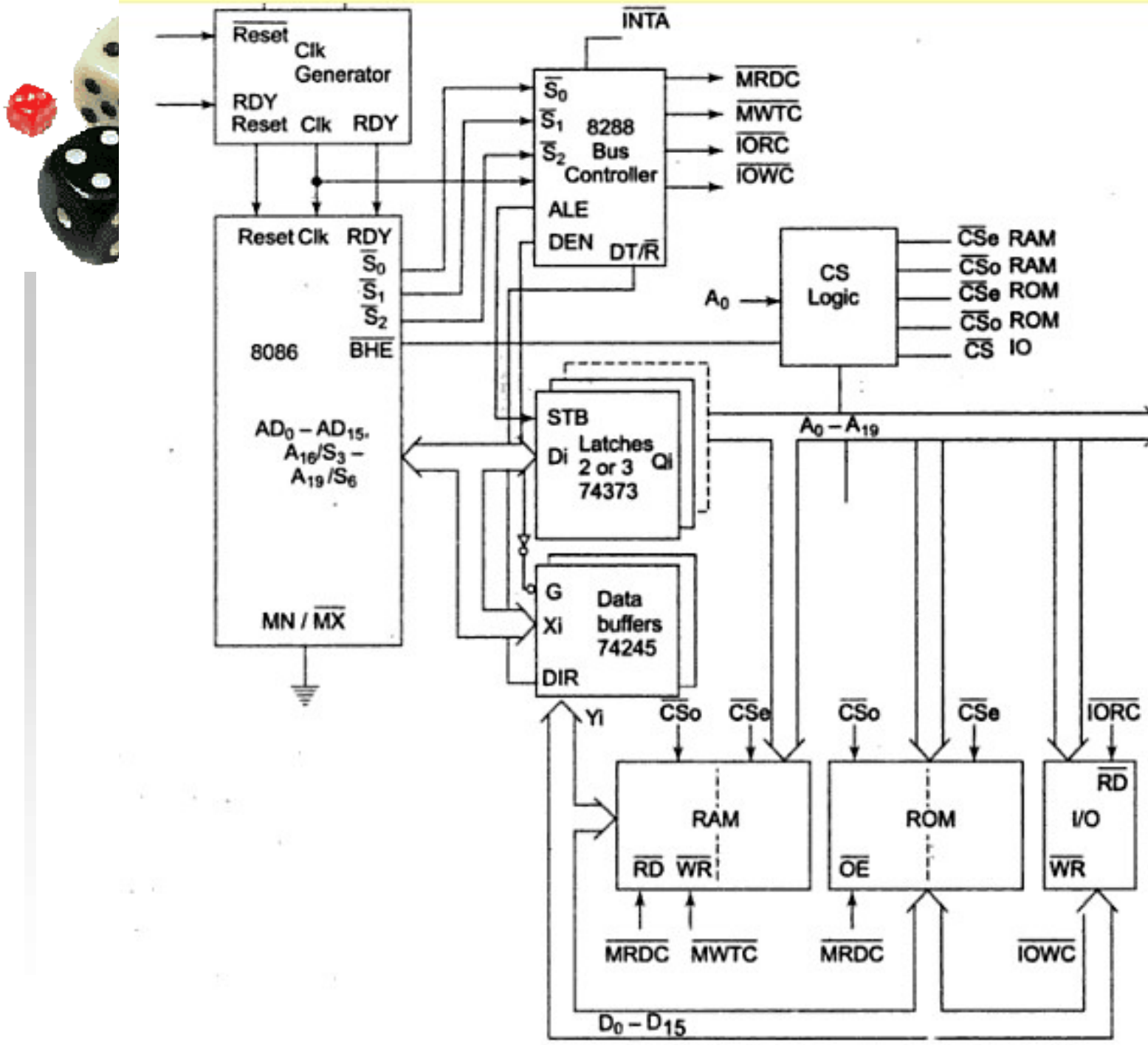
Maximum Mode Pins

Pin	Symbol	In/Out 3-State	Description
24,25	QS1,QS0	O	Reflects the status of the instruction queue. This status indicates the activity in the queue during the previous clock cycle - see Chap. 11.
26,27,28	$\overline{S0}$,$\overline{S1}$,$\overline{S2}$	O-3	Indicates the type of transfer to take place during the current bus cycle:

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Inactive - passive

(1 represents high and 0 represents low.) The status becomes active prior to the beginning of a bus cycle and returns to inactive during the later part of the cycle.

29	$\overline{LOCK}$	O-3	Indicates the bus is not to be relinquished to other potential bus masters. It is initiated by a LOCK instruction prefix and is maintained until the end of the next instruction - see Chap. 11. It is also active during and between the two $\overline{INTA}$ pulses.
30	$\overline{RQ/GT1}$	I/O	For inputting bus requests and outputting bus grants.
31	$\overline{RQ/GT0}$	I/O	Same as $\overline{RQ/GT1}$ except that a request on $\overline{RQ/GT0}$ has higher priority.


Reset
Clk Generator
RDY
Reset Clk RDY
INTA
S0
S1
S2
8288 Bus Controller
ALE
DEN
DT/R
MRDC
MWTC
IORC
IOWC
Reset Clk RDY
S0
S1
S2
8086
BHE
A0
CS Logic
CSe RAM
CSo RAM
CSe ROM
CSo ROM
CS IO
STB
Di
Latches 2 or 3 74373
Qi
A0 – A19
AD0 – AD15,
A16/S3 –
A19/S6
G
Xi
Data buffers 74245
DIR
MN / MX
Yi
CSo
CSe
CSo
CSe
IORC
RD
RAM
RD WR
ROM
OE
I/O
WR
MRDC
MWTC
MRDC
IOWC
D0 – D15

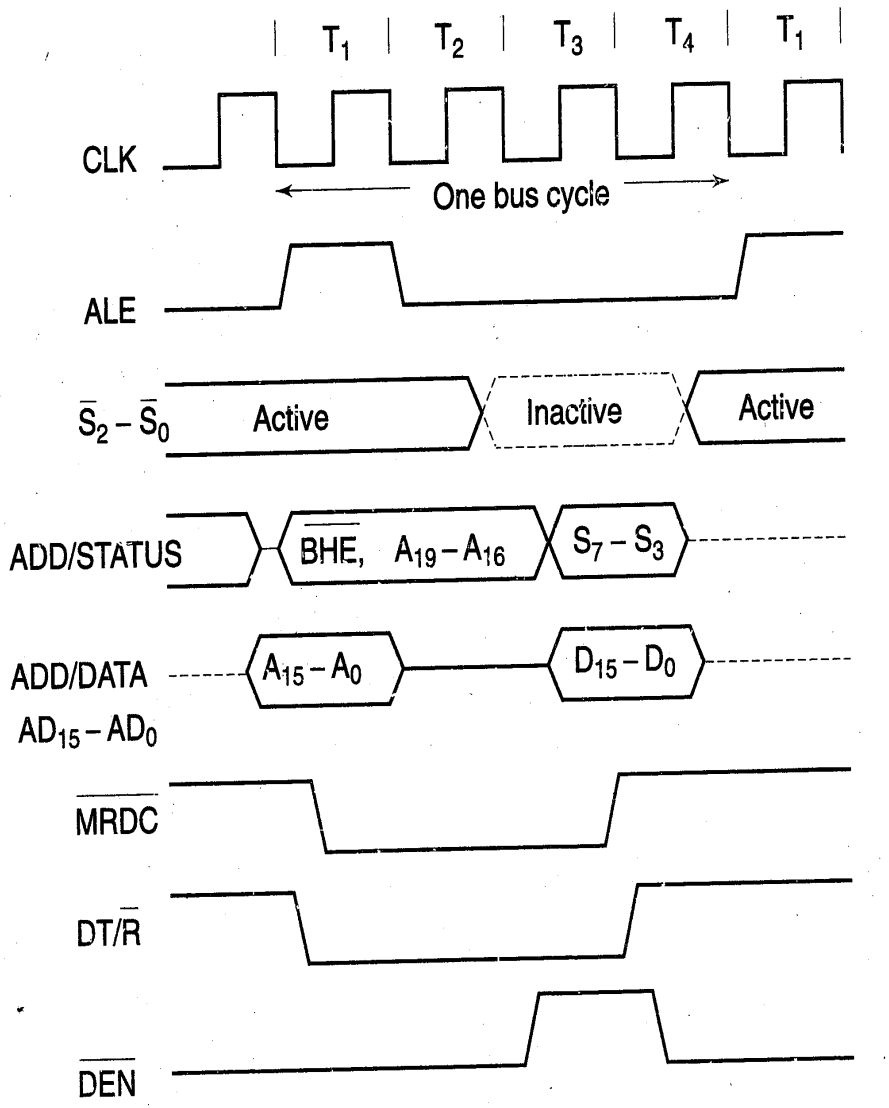


Fig. 1.11(a) *Memory Read Timing in Maximum Mode*

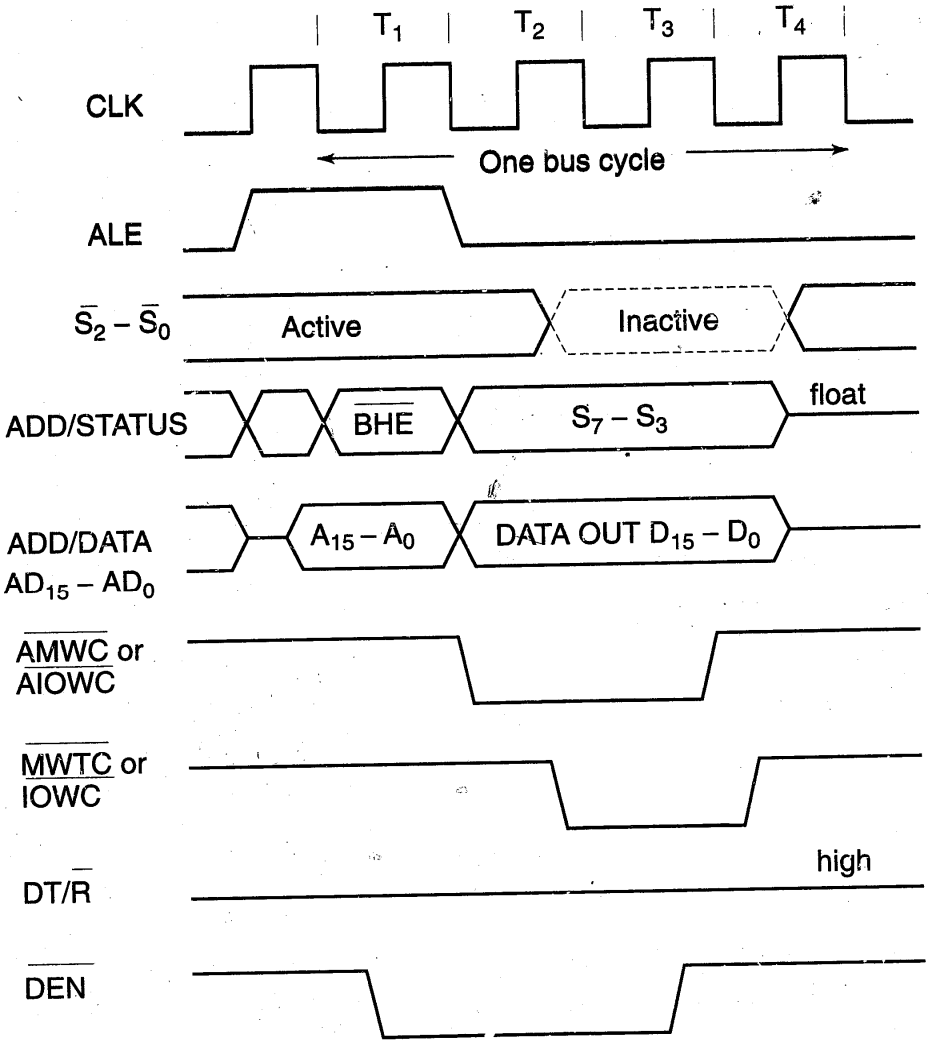


Fig 1.11(b) *Memory Write Timing in Maximum Mode*