8086 – Signal Description

By,

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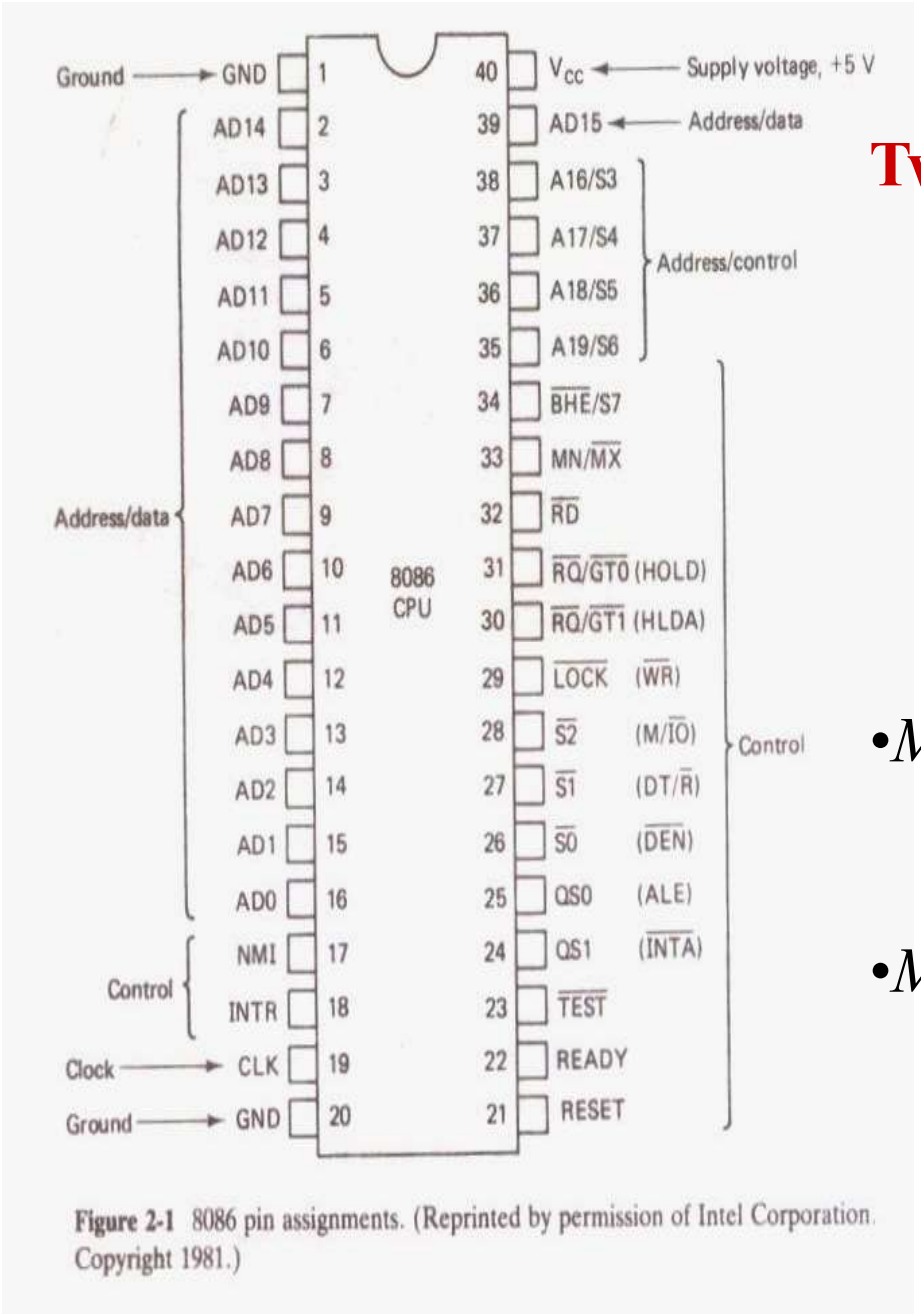

Figure 2-1 8086 pin assignments. (Reprinted by permission of Intel Corporation. Copyright 1981.)

Two mode working:

Pin 33- MN/MX

(pins 24 -31 differs)

- *Maximum Mode:*

  Multiprocessor mode

- *Minimum Mode:*

  Single Processor mode

3 Groups

- Common pins for min/max
- Pins in max mode
- Pins in min mode

Common Pins - Min/Max Modes

Pin(s)	Symbol	In/Out 3-State	Description
1	GND		Ground
2-16[1]	AD14-AD0	I/O-3	Outputs address during the first part of the bus cycle and inputs or outputs data during the remaining part of the bus cycle.
17	NMI	I	Nonmaskable interrupt request - positive-going edge triggered.
18	INTR	I	Maskable interrupt request - level triggered
19[2]	CLK	I	Clock - 33% duty cycle, maximum rate depends on CPU model 5 MHz for 8086 8 MHz for 8086-2 10 MHz for 8086-1

Common Pins - Min/Max Modes

20	GND		Ground
21	RESET	I	Terminates activity, clears PSW, IP, DS, SS, ES, and the instruction queue, and sets CS to FFFF. Processing begins at FFFF0 when signal is dropped. Signal must be 1 for at least 4 clock cycles.
22	READY	I	Acknowledgment from memory or I/O interface that CPU can complete the current bus cycle.
23	$\overline{\text{TEST}}$	I	Used in conjunction with the WAIT instruction in multiprocessing environments. A WAIT instruction will cause the CPU to idle, except for processing interrupts, until a 0 is applied to this pin - see Chap. 11.
24-31	-	-	Definition depends on mode - see Figs. 8-3 and 8-8.
32	$\overline{\text{RD}}$	O-3	Indicates a memory or I/O read is to be performed.
33	MN/$\overline{\text{MX}}$	I	CPU is in minimum mode when strapped to +5 V and in maximum mode when grounded.
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Common Pins - Min/Max Modes

34[3]	$\overline{BHE}$/S7	O-3	If 0 during first part of bus cycle this pin indicates that at least one byte of the current transfer is to be made on pins AD15-AD8; if 1 the transfer is made on AD7-AD0. Status S7 is output during the latter part of bus cycle, but, presently, S7 has not been assigned a meaning.
35-38	A19/S6-A16/S3	O-3	During the first part of the bus cycle the upper 4 bits of the address are output and during the remainder of the bus cycle status is output. S3 and S4 indicate the segment register being used as follows:

S4	S3	Register
0	0	ES
0	1	SS
1	0	CS or none
1	1	DS

S5 gives the current setting of IF.
S6 is always 0.

39[1]	AD15	I/O-3	Same as AD14-AD0
40	VCC	-	Supply voltage - +5 V ± 10%

Pins – Min Mode

Pin	Symbol	In/Out 3-State	Description
24	$\overline{\text{INTA}}$	O-3	Indicates recognition of an interrupt request. Consists of two negative going pulses in two consecutive bus cycles.
25	ALE	O	Outputs a pulse at the beginning of the bus cycle and is to indicate an address is available on the address pins.
26	$\overline{\text{DEN}}$	O-3	Output during the latter portion of the bus cycle and is to inform the transceivers that the CPU is ready to send or receive data.
27	DT/$\overline{\text{R}}$	O-3	Indicates to the set of transceivers whether they are to transmit (1) or receive (0) data.
28[1]	M/$\overline{\text{IO}}$	O-3	Distinguishes a memory transfer from an I/O transfer. For a memory transfer it is 1.
29	$\overline{\text{WR}}$	O-3	When 0, it indicates a write operation is being performed. It is used in conjunction with pins 28 (M/$\overline{\text{IO}}$) and 32 ($\overline{\text{RD}}$) to specify the type of transfer
30	HLDA	O	Outputs a bus grant to a requesting master. Pins with tristate gates are put in high impedance state while HLDA=1.
31	HOLD	I	Receives bus requests from bus masters. The 8086/8088 will not gain control of the bus until this signal is dropped.

[1]For the 8088, the symbol is IO/$\overline{\text{M}}$ and a 1 indicates an I/O transfer.

Pin	Symbol	In/Out 3-State	Description
24,25	QS1,QS0	O	Reflects the status of the instruction queue. This status indicates the activity in the queue during the previous clock cycle - see Chap. 11.
26,27,28	$\overline{S0}$,$\overline{S1}$,$\overline{S2}$	O-3	Indicates the type of transfer to take place during the current bus cycle:

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Inactive - passive

(1 represents high and 0 represents low.) The status becomes active prior to the beginning of a bus cycle and returns to inactive during the later part of the cycle.

29	$\overline{LOCK}$	O-3	Indicates the bus is not to be relinquished to other potential bus masters. It is initiated by a LOCK instruction prefix and is maintained until the end of the next instruction - see Chap. 11. It is also active during and between the two $\overline{INTA}$ pulses.
30	$\overline{RQ/GT1}$	I/O	For inputting bus requests and outputting bus grants.
31	$\overline{RQ/GT0}$	I/O	Same as $\overline{RQ/GT1}$ except that a request on $\overline{RQ/GT0}$ has higher priority.

Pins
Max Mode