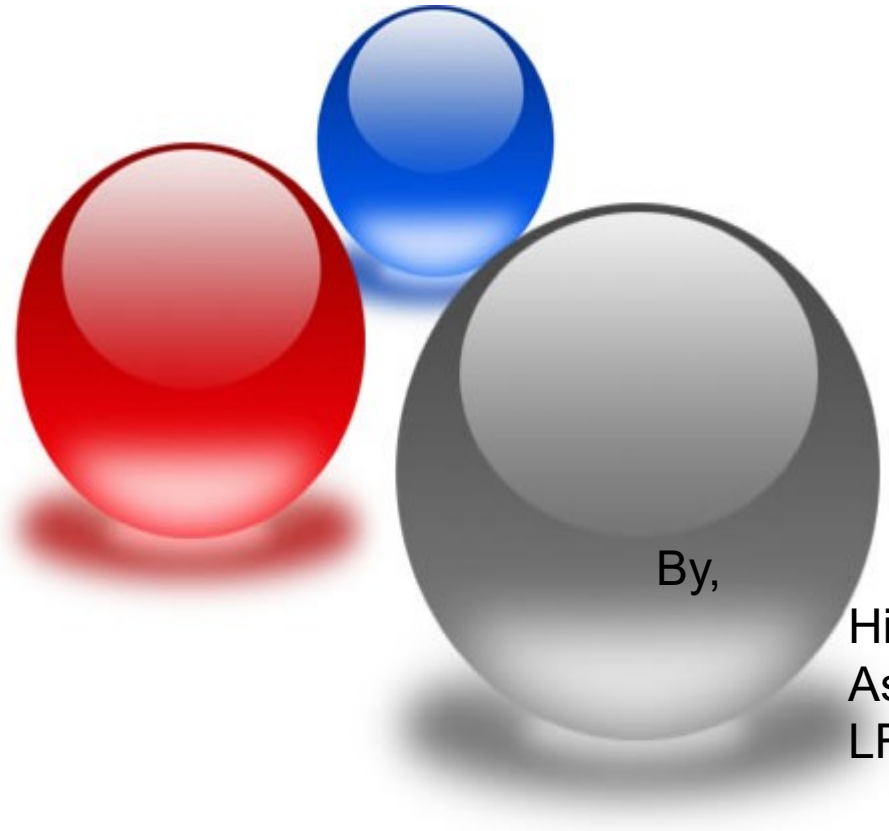
More about 8086

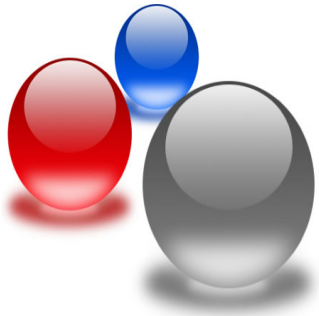


By,

Hitha Paulson
Assistant Professor, Dept of Computer Science
LF College, Guruvayoor

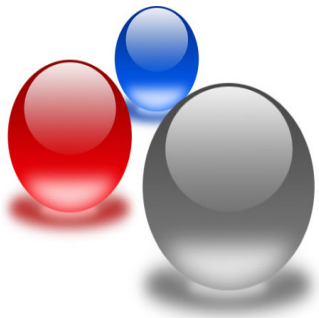
Physical Memory Organization

- Odd bank and Even bank
- BHE & A0
- A Word may be
  - 2 operands
  - 2 opcodes
  - 1 operand & 1 opcode
- Cycles needed

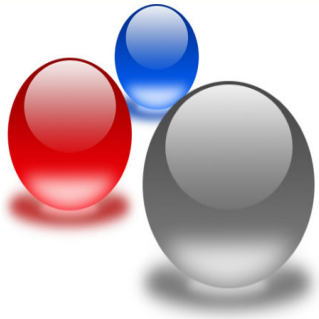


Physical Memory Organization

- Certain locations in memory are reserved for some operations.
- FFFF0H to FFFFFH – for operations including jump to initialization program and I/O processor initialization.
- 00000H to 003FFH – interrupt vector table
  - 256 interrupts (4 byte address- CS + IP)



General Bus Operation



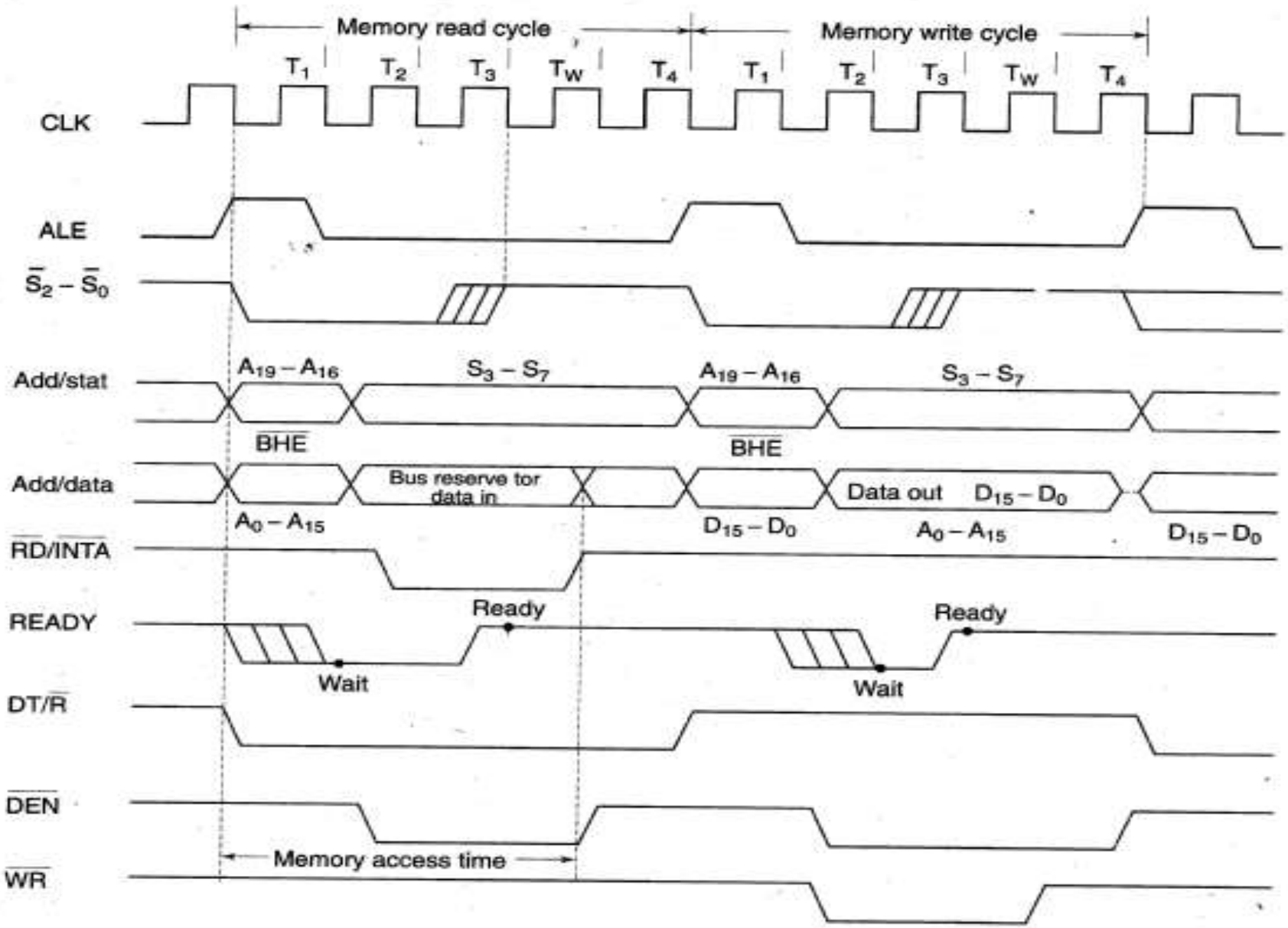
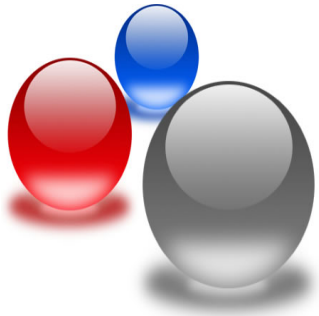


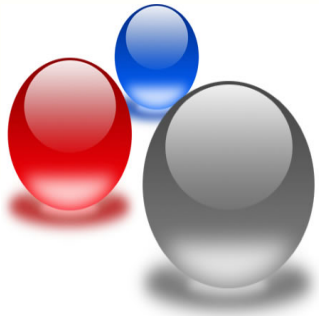
Fig. 1.7 *General Bus Operation Cycle in Maximum Mode*

I/O Addressing Capability

- 8086 can address up to 64K I/O byte registers or 32 K word registers.
- Only 16 bit IO address supported for I/O devices.
- A0 to A15 used as address bus (other four bits 0)
- DX – I/O address pointer
- Memory mapped I/O & I/O mapped I/O

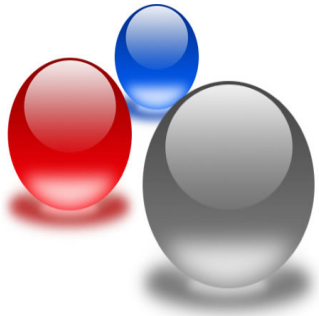


Special Processor Activities

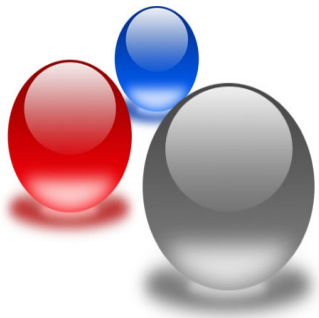


1.Processor Reset and Initialization

- RESET Pin – should be high for at least 4 Clock Cycles
- Reset still 0 applied to it.
- Reset sequence starts on negative edge.
- It takes 10 clock cycles
  - All internal registers set to 0000H
  - CS set to FFFFH, IP to 0000H
  - It is EPROM with memory address(FFFF0H to FFFFFH)



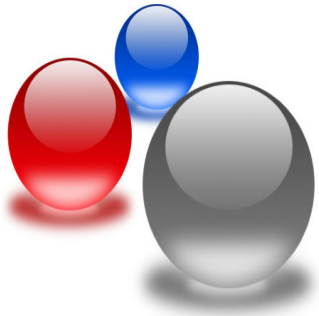
- For NMI it should appear after second clock cycle during reset initialization



2. HALT

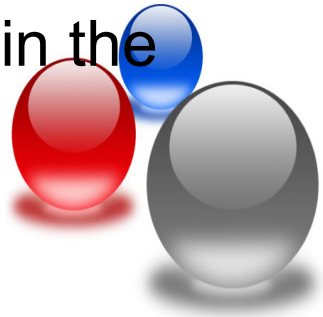
- HLT instruction
- Enter to halt state in 2 ways
- Minimum mode
  - Issues ALE pulse, but not issue any control signal
- Maximum mode
  - Puts Halt status on s0,s1,s2. ALE followed by no signal.

- HOLD request not served
- Interrupt served



3. TEST Signal

- When WAIT instruction encoders.
  - Preserves all register values
  - Enters wait state and checks for TEST signal to go slow.
  - If low working continues, low for atleast 5 clock cycles.
- HOLD request served
- If Interrupt occurs , it fetches wait instruction once more executes it and serves the interrupt.
- After that it fetches wait instruction and continues in the state



Deriving System Bus

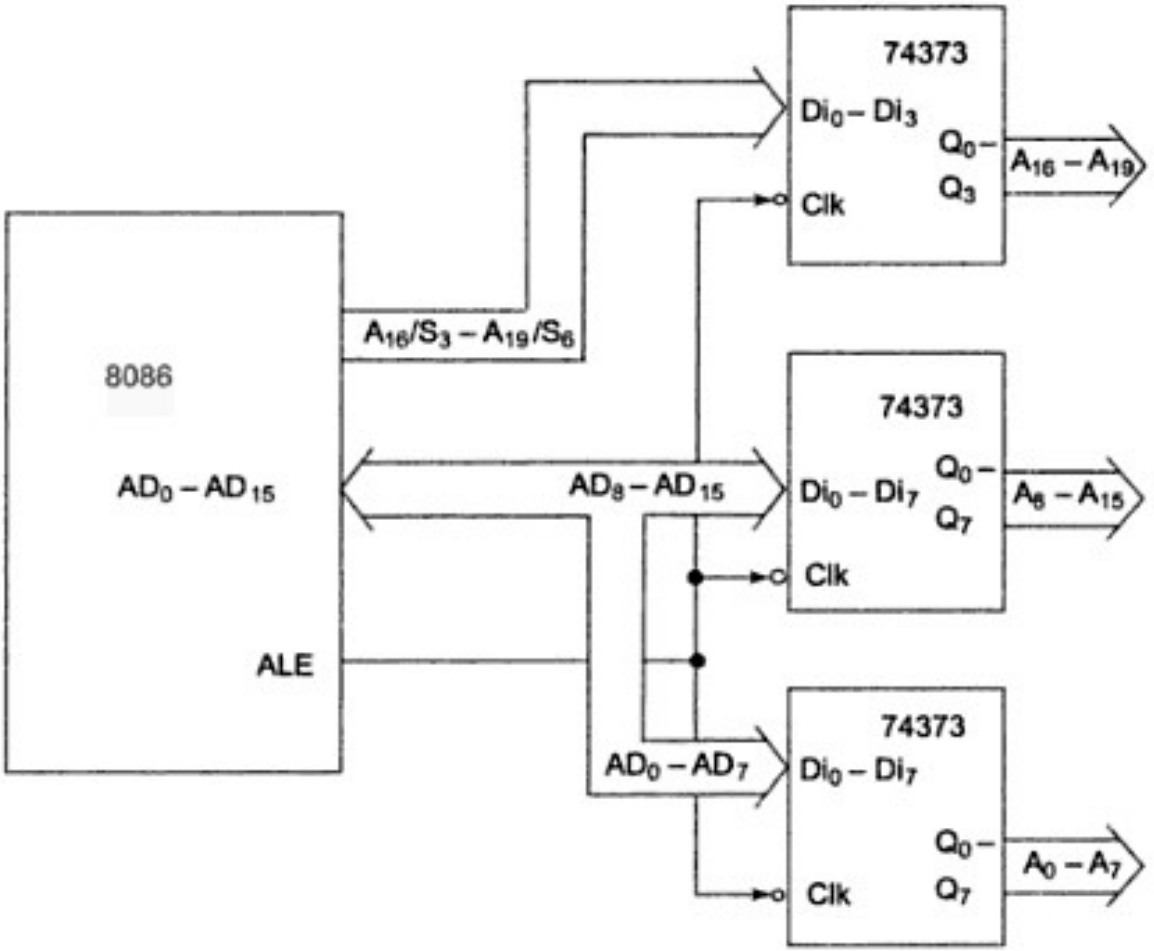
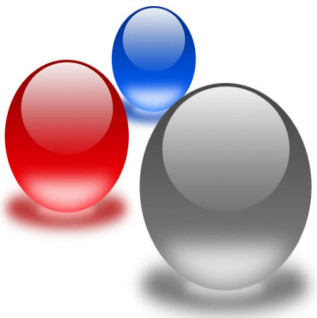


Fig.1.10 *Latching 20-Bit Address of 8086*



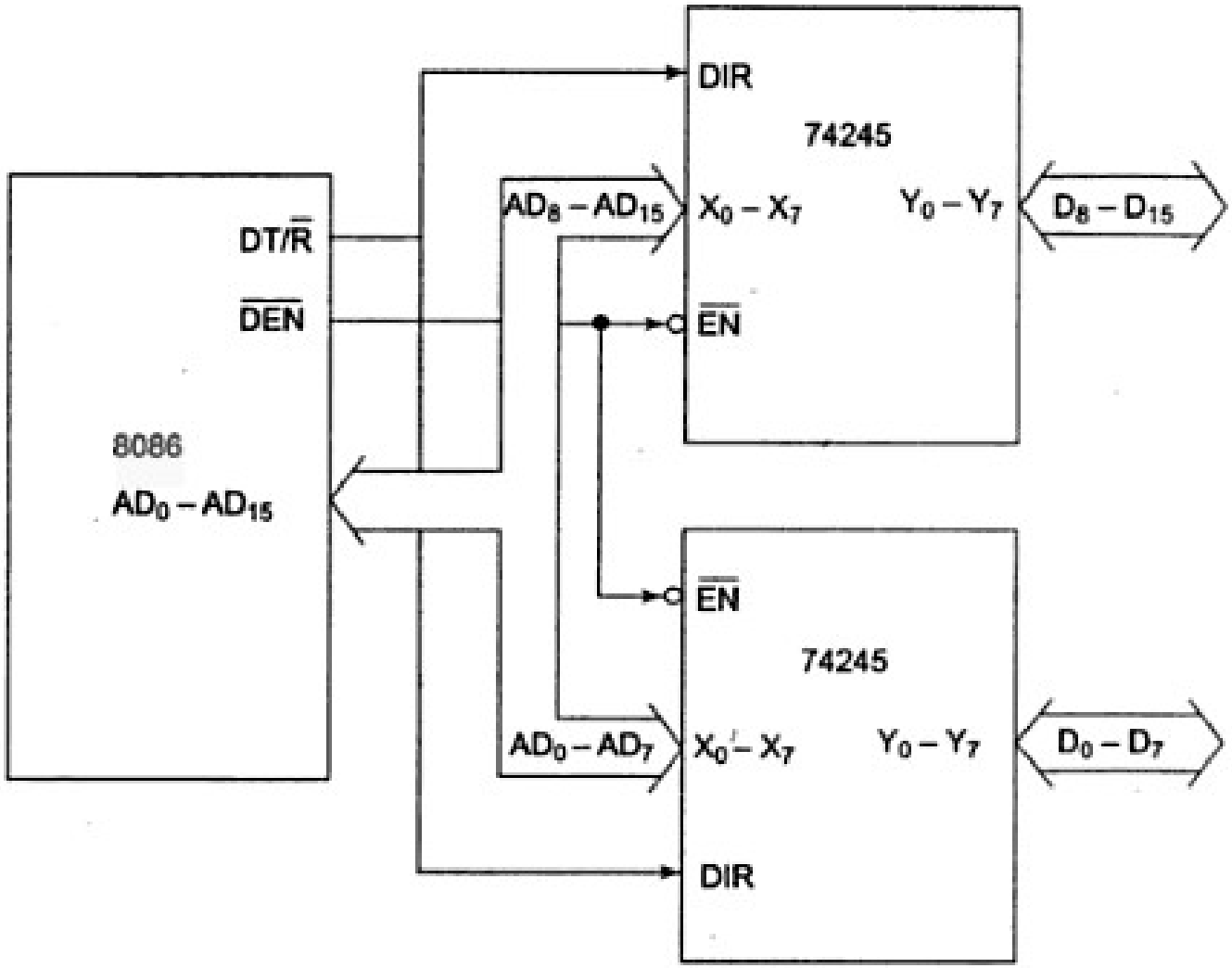


Fig. 1.11 *Buffering Data Bus of 8086*

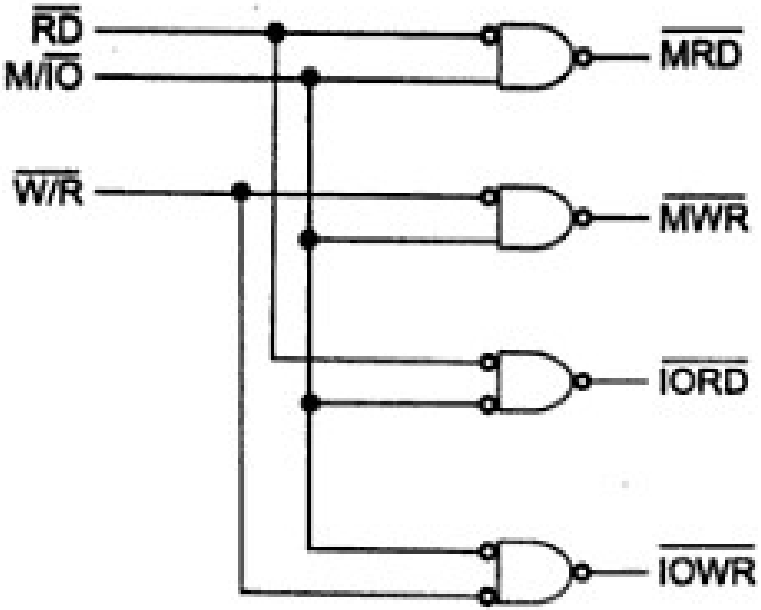


Fig.1.12 (a) *Deriving 8086 Control Signals*

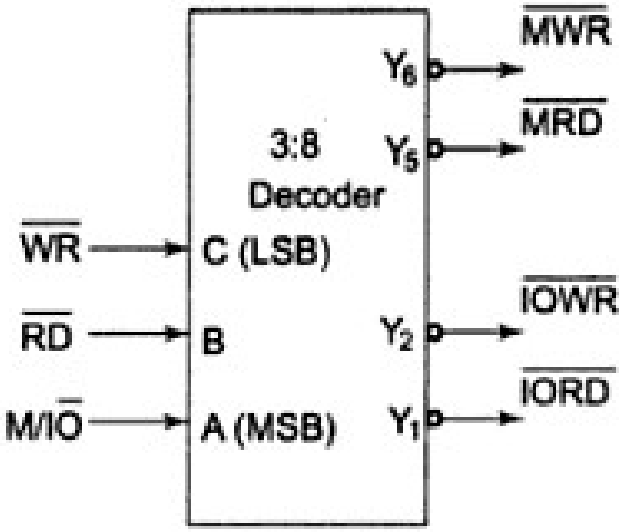


Fig.1.12 (b) *Deriving 8086 Control Signals*